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Low-temperature Metal Bonding for Optical Device Packaging

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Abstract—Low-temperature solid-liquid interdiffusion (SLID) bonding is an attractive alternative for the packaging of optical devices. It reduces global residual stress build up caused by differences in coefficient of thermal expansion (CTE) at elevated temperatures. This work applied the Cu-Sn-In-based SLID bonding method to bond silicon and optically transparent materials at 200 °C. Experimental results show a successful bonding with minor unavoidable misalignment from the CTE mismatch and major misalignment from the bonding alignment process. Microstructural analysis shows the intermetallic compound consists only of $\text{Cu}_6(\text{Sn},\text{In})_5$ on the bond that is thermally stable up to 600 °C.

Keywords—Optical device packaging, Low-temperature Bonding, Intermetallic Compound

I. INTRODUCTION

Glass is a material of interest for packaging optical MEMS devices, such as micro-mirrors and image sensors. It offers a wide range of wavelength transparency, low production cost, high chemical stability and low electrical parasitics element [1]. At present, there are some wafer-level glass bonding technologies, such as glass frit and anodic bonding [2]. However, their processes are limited by high-temperature (>350 °C) requirement, which induces thermo-mechanical stress in the device due to variations in the coefficient of thermal expansion (CTE). These residual stresses exist locally, between the substrate and bond, and globally, between the bonded substrates [3], [4]. Furthermore, high-temperature processes are also incompatible with temperature-sensitive materials, such as organic-based lighting or sensors [5].

The solid-liquid interdiffusion (SLID) bonding method is a wafer-level metal bonding process that could be done at a low temperature [3], [6]. The process involves the interdiffusion of base metals to form an intermetallic compound (IMC) that results in a bonded structure with a higher remelting temperature than the bonding temperature [7], [8]. Furthermore, it is compatible with hermetic encapsulation and vertical interconnects, which are very

attractive for 3D MEMS development, as illustrated in Fig. 1 [9]–[12].

Recent findings have shown that SLID bonding temperature could be further reduced to the range of 200 °C with the addition of indium to the widely used Cu-Sn system [3]. The low-processing temperature could further minimize the thermomechanical stress that arises from CTE mismatch during the bonding process [13]. Thus, the low-temperature SLID (LT-SLID) bonding process could become a solution for robust packaging for thermally sensitive optical devices and contributes minimally to local and global residual stresses.

This study aims to demonstrate the possibility of the LT-SLID bonding process for glass-like materials with large CTE differences with silicon. Results from the experimental work have demonstrated wafer-level bonding of silicon to optically transparent materials with the LT-SLID process.

II. METHODOLOGY

In this work, the low temperature SLID bonding process based on the Cu-Sn-In ternary was tested to bond 4-inch silicon wafer with several optically transparent wafers of the same size with properties listed in Table 1.

TABLE I. PROPERTIES OF WAFERS SUBSTRATE USED IN THE LT-SLID PROCESS

Material	CTE* (K^{-1})	Young's modulus (GPa)	Density (g/cm^3)	Thickness (μm)
Fused Silica (JGS2) [14]	5.5 E-7	71.7	2.20	500
Borosilicate (BOROFLOAT® 33) [15]	3.25 E-6	64	2.23	500
Borosilicate (D263) [16]	7.2 E-6	72.9	2.51	500
Silicon <100> n-type [17]	2.6 E-6	165	2.33	380

*Linear coefficient of thermal expansion measured up to 300 °C

Fig. 1. Illustration of optical MEMS packaging cross-section with SLID bonding process including a TGV.

The metal bonds were fabricated with square-shaped microbumps composed of copper, tin, and indium metal layers as a medium. The microbumps were distributed across the wafer surface in a 5 mm x 5 mm chip. Each chip contains several microbumps of same size varied between 10, 25, 50, 100 or 250 μm , as illustrated in Fig. 2. The chips were designed to have the same total metal bonds surface area despite the sizes, to ensure homogenous parameter during metal deposition and bonding process. In total, each wafer has a bonding area of 2.52 cm^2 , implying 252 chips on the 4-inch wafer. The detailed fabrication process flow is illustrated in Fig 3.

Fig. 2. Microbumps design on the 4-inch wafer.

The process started with sputter deposition of 20 nm TiW adhesion layer, followed by 100 nm Cu seed layer on each substrate surface. Then thick photoresist mask with square cavities was developed through the lithography process with AZ15nXT photoresist. The metals were deposited with electrochemical deposition method in a fountain based electroplating set-up. Copper with 3.5 μm thickness was deposited with NB SEMIPLATE CU 100 electrolyte, current density of 15 mA/cm^2 , and regulated at 28 $^{\circ}\text{C}$ temperature. Subsequently, 1.5 μm thick tin was deposited in a similar set-up with NB SEMIPLATE SN 100 at room temperature with a current density of 15 mA/cm^2 . The indium layer was deposited last using indium sulfamate plating bath at room temperature with current density of 10 mA/cm^2 and

Fig. 3. Process flow of LT-SLID bonding process: (a) Sputtering of TiW/Cu seed layer, (b) photoresist spinning, (c) photoresist development, (d) electrodeposition of copper (orange), (e) tin (grey), (f) indium (purple), (g) resist removal, (h) TiW/Cu seed layer wet etching, (i) bonding process at 200 $^{\circ}\text{C}$, (j) SLID bond formed with intermetallic compound (light green).

controlled pH of 1.6. After the metal depositions, the photoresist mask was stripped in NI555 resist strip, followed by wet etching of excess Cu seed and TiW layers.

The bonding process was completed in AML wafer bonder with glass wafers positioned at the movable bottom platen and silicon wafer fixed at the upper platen. The microbumps were aligned and pre-heated to 100 $^{\circ}\text{C}$ prior to being in contact. The wafers are brought into contact with 4.3 kN uniaxial contact force from the bottom platen and heated up to 200 $^{\circ}\text{C}$ with a heating rate of 10 $^{\circ}\text{C}/\text{min}$. After 1 hour of holding time at 200 $^{\circ}\text{C}$, the contact force was released, and the temperature was brought down to 65 $^{\circ}\text{C}$ with a slow

Fig. 4. Respectively images of (a, d, h) LT-SLID bonded wafers before dicing process, optical micrograph of (b, e, i) 50, (c, f, j) 100, and (d, g, k) 250 μm bump for: Si-Fused Silica, Si-BOROFLOAT®33, and Si-D263, respectively.

Fig. 5. Misalignment direction after the bonding process (hollow+: glass, filled +: Silicon) for (a)Si-Fused Silica, (b) Si-BOROFLOAT®33, and (c)Si-D263®.

cooling rate of 1 °C/min before the bonded pair was taken out of the chamber.

After the bonding process, the bonds on the wafers were characterized using an optical microscope from the glass side. The wafers were then subjected to dicing procedure for microstructure analysis of the bond cross-section with SEM and EDS. A successfully bonded Si-Si bonded pair using the same procedure is used as a reference sample for the microstructural analysis.

III. RESULTS AND DISCUSSIONS

The bonding results for the silicon to glass wafers are presented in Fig. 4. Birefringence patterns can be observed on the glass substrates, attributing to residual stress from the bonding process. Magnification image of the 250 μm bump for each pair shows squeeze out, which indicates a high concentration of melted tin and indium [3], [7]. Additionally, misalignment is observed on all the microbumps size and more evident on the smaller bumps. Major misalignments ($>20 \mu\text{m}$) can occur during the bonding process due to the poor aligning process, which could be controlled. However, minor misalignments are caused by the different CTE of the substrates used in the bonding process which is unavoidable and seems difficult to control. Fig. 5 summarizes the misalignment observed on the wafer based on the different Si-glass pairs. Major misalignment, such as rotational misalignment in 5(a) and 5(b), are caused by the aligning process. However, minor misalignments caused by the CTE differences can be observed on all the bonded wafers. Si-Fused Silica pair in Figure 5a shows misalignment moving

Fig. 6. Cross section images of bonded (a)Si-Si, (b)Si-Fused Silica, (c) Si-BOROFLOAT®33, and (d)Si-D263® 250 μm microbumps.

towards the center of the wafer as fused silica has a smaller CTE compared to silicon. On the other hand, Si-BOROFLOAT®33 and Si-D263® misalignment are shown moving towards the edge of the wafer as the glass CTEs are larger than silicon.

Assuming the expansion is radially uniform towards the edge. The amount of misalignment from the center towards the edge can be estimated using:

$$\Delta L = L_0(\alpha_1 - \alpha_2)\Delta T \quad (1)$$

Where ΔL is the misalignment value, L_0 is the radius of the wafer, α_1 and α_2 are the thermal expansion coefficients, and ΔT is the temperature difference. A rough estimation of the minor misalignment based on the experiment condition for Si-Fused Silica, Si-BOROFLOAT®33, and Si-D263® are 1.8, 0.5, and 4 μm , respectively. Consequently, these values show the allowable minimum feature size required for a successful bonding process of materials with high CTE contrast.

Cross-sectional observations of the 250 μm bump of bonded samples are shown in Fig. 6 along with bonded Si-Si reference sample as a comparison. The SEM images show a distinct feature of an IMC layer sandwiched between remaining copper layers that were not consumed during the IMC formation. The thickness of bonded layers varies depending on the metal layer thickness deposited before the bonding process.

Fig. 7 summarizes the total thickness of deposited Cu-Sn-In metal layers on each silicon and their respective glass cap wafers before and after the bonding process. Prior to the bonding, there are roughly more than 3.5 μm copper on each side of the substrates accounting for copper total thickness of 7.8-8.4 μm . After the bonding process, the copper thickness was reduced to less than half of the initial value due to the diffusion process into the In-Sn melt to form the $\text{Cu}_6(\text{Sn},\text{In})_5$ phase. Furthermore, it was observed in the samples that the amount copper consumed is proportional to the thickness of deposited tin and indium, such as in bonded Si-D263®.

The thickness of initial tin and indium metal layers varied significantly between each pair of samples due to the electroplating condition. However, the ratio of tin to indium on each pair was kept at 1:1 for optimal bonding conditions.

Fig. 7. Cu-Sn-In metal layers thickness before and after the bonding process.

The indium and tin layers have a total thickness of 5.5 - 7.2 μm , which were reduced to a single IMC layer with a total thickness of roughly 4 - 5.6 μm after the bonding process. Overall, there is a significant reduction in the microbumps total thickness after the bonding process, which can be attributed to the squeeze-out process and volume shrinkage during the formation of the IMC.

The IMC existing in the bond were further studied with EDS compositional analysis. Table 2 summarizes the result of the elemental composition of the IMC observed in the SEM image. The bonded Si-Si reference sample shows a composition of 54% Cu, 22% Sn, and 24% In, which strongly correlates to the elemental composition of $\text{Cu}_6(\text{Sn},\text{In})_5$. The bonded Si-Fused Silica, Si-BOROFLOAT®33, and Si-D263® samples exhibited a similar elemental composition of 57% Cu, 21.5% Sn, and 21.5% In. This indicated the bonding process at 200 °C was successful to form a good thermally stable bond up to 600 °C [3], [18].

TABLE II. EDS COMPOSITIONAL ANALYSIS OF IMC AFTER BONDING PROCESS

Element	At%			
	Si – Si reference sample	Si – Schott D263®	Si – BOROFLOAT® 33	Si – Fused Silica
Cu	54.1 ± 0.1	57.8 ± 0.3	56.9 ± 1	58 ± 0.3
In	22.3 ± 0.4	20.5 ± 1	21.6 ± 2.7	21.5 ± 0.4
Sn	23.6 ± 0.4	21.7 ± 1.2	21.5 ± 2.7	20.5 ± 0.5

IV. CONCLUSION

Successful wafer-level low-temperature metal bonding for silicon and optically transparent materials with high CTE variations have been demonstrated in this work. Microstructural characterization on bonded Si-Fused Silica, Si-BOROFLOAT®33, and Si-D263® samples show distinct features of intermetallic compound layer sandwiched between copper layers. The IMC consists solely of $\text{Cu}_6(\text{Sn},\text{In})_5$ phase indicating a thermally stable bond up to 600 °C. This result opens new opportunities for low thermal stress bonding silicon to glass-like materials for optical device packaging. Further studies will include thorough microstructural analysis and phase study in addition to reliability study of the bonds.

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