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A Compact Low-Power 140-GHz Low-Noise Amplifier with 19-dB Gain and 7-dB NF

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Abstract—This paper describes the design of a 140-GHz low-noise amplifier in 130-nm SiGe BiCMOS technology. The circuit is aimed for a high integration-density imaging radiometer, where several receivers are integrated on the same die. Thus, we particularly focus on minimizing the die area and power consumption. The two-stage amplifier is composed of cascode stages with gain boosting base resonators. The performance of a single cascode stage is optimized by correctly sizing the base resonator to avoid instability and optimizing the compact transistor layout without typically used interstage matching between the cascode stages. The circuit features gain of 19 dB at 140 GHz, and noise figure of 7 dB, while consuming only 15 mW with the supply voltage of 2 V and occupying a die area of 0.1 mm².

Index Terms—Low-noise amplifier, radiometer, phased array, BiCMOS, SiGe, HBT

I. INTRODUCTION

The exploitation of millimeter-wave frequencies has grown steadily during the recent years. Radars, sensors, security scanning, active and passive imaging, and ultra-high bandwidth communication are common examples. Many of these applications, such as automotive radars, were first developed for sub-100 GHz frequencies, but now research is heading for higher frequencies, and atmospheric window at 140 GHz is one such regime. Second megatrend on millimeter-wave IC development is the expansion of complexity, and recently several highly complicated transceivers have been demonstrated, such as [1]–[5].

A radiometer is one of the emerging devices, which will benefit of the integration of sub-THz circuits on a single die. The radiometer captures an image at sub-THz region by using several concurrent receivers. Hence, in the development of a radiometer, one target is to integrate several receiver chains in the same die within a close proximity of an antenna array.

A low-noise amplifier (LNA) is an essential building block in millimeter-wave receivers, since received power level is often low, and thus high sensitivity is needed. In a radiometer IC multiple receiver units will be implemented on a same die and therefore a small die area and low power consumption become important design targets. At 140 GHz typical $\lambda/2$ antenna spacing is only about 1 mm giving opportunity for close proximity of die and antenna interfaces, while typical system design indicates that LNA gain should be in range of 15-20 dB.

Fig. 1. The schematic of a two-stage cascode LNA. BIAS CM refers to the biasing current mirror.

With the aforementioned motivation in mind, in this paper we present a two-stage cascode LNA that features gain of 19 dB at 140 GHz, and noise figure of 7 dB, while consuming only 15 mW and occupying a small die area of 0.1 mm². In Section II we describe the structure of our amplifier and we focus on the main theoretical aspects regarding the LNA design. In this LNA inductive feedback on the bases of cascode transistors is utilized to increase gain. An analysis and design guidelines are presented in Section II-A. In addition, an analysis of the parasitic capacitance of the connection between the cascoded transistors is presented in Section II-B. Section III describes the actual circuit and layout design. Specifically we describe all the essential elements and interconnections of the circuit that have been verified with electromagnetic field simulations. In addition, significance of high-frequency design methodology is discussed, and its utilization with our design is specified. In Section IV we represent the simulation results and Section V concludes the paper with a summary of main outcomes.

II. OPERATION PRINCIPLES

The designed LNA is a two-stage cascode amplifier as depicted in Fig. 1. The cascode transistors Q_2 and Q_4 reduce

the Miller effect, since the outputs of the first and second stage are connected to the ground through the parasitic base-to-collector-capacitance of Q_2 and Q_4 . As a consequence, the cascode transistors expand the gain bandwidth and improve reverse isolation. However, Q_2 and Q_4 also introduce additional noise sources to the circuit resulting in increased noise figure.

The gain of the cascode amplifier was further improved by adding a tiny inductor to the bases of Q_2 and Q_4 . The base inductance L_b creates positive feedback by feeding a part of the signal at Q_2 and Q_4 bases back to the emitters through the parasitic base-to-emitter-capacitance.

A crucial element to consider with the design of a cascode amplifier is a parasitic capacitance C_{par} between the cascoded transistors. The capacitance C_{par} is created by the connection of the collector of the common emitter (CE) -transistor and the emitter of the common base (CB) -transistor, and it should be minimized or resonated out, so that the gain of the amplifier does not degrade. Here we focus on the method of minimizing C_{par} with a sophisticated layout, because our main design target was to implement an LNA with a minimized die area and power consumption.

A. Base Resonator

The effect of the base inductance L_b on the LNA performance was studied with one stage and without input and output matching. The maximum available gain (MAG) and Rollett's stability factor K were examined in order to analyze the circuit response to different L_b values.

Fig. 2 presents MAG and the stability factor K as the function of L_b at 140 GHz. The stability factor decreases as L_b increases, and eventually the amplifier becomes unstable. MAG increases along L_b until $L_b = 8$ pH, when $K < 1$ and MAG is undefined. Both MAG and K vary rapidly along L_b , which indicates high sensitivity to the L_b value.

The base inductance value was selected to be 6 pH for the designed LNA. Although the highest MAG value could be achieved with $L_b = 8$ pH, the amplifier has a risk of becoming unstable due to inaccuracies in simulations.

The effect of L_b on the amplifier gain can also be studied by determining the output impedance Z_{out} of the cascode amplifier. By representing the transistors with the base-to-emitter capacitances $C_{\pi 1-2}$, transconductances g_{m1-2} , and output resistances r_{o1-2} , Z_{out} is

$$Z_{out} = r_{o2} + \frac{g_{m2}r_{o1}r_{o2} + r_{o1}(1 - \omega^2 L_b C_{\pi 2})}{1 - \omega^2 L_b C_{\pi 2} + j\omega C_{\pi 2} r_{o1}} \quad (1)$$

and the real part of Z_{out} can be approximated as

$$Re(Z_{out}) \approx \frac{g_{m2}r_{o1}r_{o2}}{1 - \omega^2 L_b C_{\pi 2}} \quad (2)$$

As a consequence of increasing $Re(Z_{out})$, the intrinsic gain of the amplifier improves. However, if the condition $\omega^2 L_b C_{\pi 2} < 1$ is broken, the amplifier becomes unstable, since the real part of Z_{out} is negative.

Fig. 2. MAG and K as the function of L_b at 140 GHz

Fig. 3. Connections of the cascoded transistors and C_b

B. Parasitic capacitance

The effect of the base resonator and C_{par} can be analyzed by calculating the transfer function $H(j\omega) = V_{out}(j\omega)/V_{in}(j\omega)$ of the cascode amplifier from an approximated small signal equivalent circuit with the transistor base-to-emitter capacitances $C_{\pi 1-2}$, transconductances g_{m1-2} , and output resistances r_{o1-2} . The cascoded transistors are equally sized and biased, so $g_{m1} = g_{m2} = g_m$ and $r_{o1} = r_{o2} = r_o$ were assumed. Eq. 3 presents the transfer function, where $A = 1 - \omega^2 L_b C_{\pi 2}$. This can be approximated as Eq. 4, where the effect of the base resonator and C_{par} is visible.

According to Eq. 3 and Eq. 4, the effect of C_{par} on the voltage gain can be manipulated with the base resonator. If $\omega^2 L_b C_{\pi 2} = 1$, C_{par} has no effect on $H(j\omega)$. However, as it was stated in Section II-A, the amplifier may become unstable if L_b is too large.

According to schematic-level simulations with an added C_{par} between the cascoded transistors, the effect of C_{par} could be mitigated significantly with the base resonator. MAG of a cascode amplifier without L_b , and with presence of $C_{par} = 10$ fF, was simulated to be 11.8 dB at 140 GHz. With $L_b = 6$ pH, MAG = 15.4 dB, which is close to MAG = 15.7 dB when $C_{par} = 0$. For comparison, the amplifier performance was studied with a series and parallel resonator between the cas-

coded transistors. The highest MAG of 13.6 dB was achieved when a series inductance resonated with C_{par} . Compared to the base resonator, the series and parallel resonators offered inferior performance. Additionally, considering the target of minimum area consumption, the series and parallel resonators would have required a large die area compared to the base resonator.

III. CIRCUIT DESIGN

Fig. 1 presents the detailed schematic of the designed LNA. The supply voltage V_{DD} is 2 V, and the LNA is biased with a current mirror with degenerated emitters on the bias circuit and LNA sides for matched biasing. The emitters of the common-emitter transistors of the LNA are degenerated with resistors R_e and capacitors C_e in order to reduce sensitivity of the gain response to variations of the bias currents.

The first and second stages have separate bias circuits due to the possibility of tuning biasing of the stages independently. When the designed LNA is used in a receiver, digital current control (IDAC) will be utilized in biasing.

The power consumption was minimized by decreasing the transistor collector DC-currents by studying the unity current gain frequency response of the cascode amplifier. Therefore, the LNA performance remained sufficient despite of decreased bias currents.

In the designed LNA, the base inductances L_{b1-2} are implemented as the parasitic inductances of the connections between the CB-transistor bases and the base capacitors C_{b1-2} , which provide RF ground for the signal. The LNA stability is sensitive to the L_b value, so the base connection parasitics provide sufficient inductance.

The topmost metal was utilized as signal transmission lines, which are 8 μm wide. The transmission lines T_{1-2} realize the input matching circuit and the lines T_{5-7} the output matching circuit. Both input and output are matched to 50 Ω . The reflection coefficient at the input for the optimum noise performance was determined, and the matching circuit was tuned according to it.

Since the main target of the design was minimizing the layout area, the LNA components were placed as close to each other as possible. Matching between the first and second stage was studied, and the load T_3 of the first stage provided sufficient matching. As a consequence, the stages could be positioned close to each other without additional matching circuits. The length and position of T_3 were modified to improve noise performance.

However, if adjacent long signal lines are placed close to each other, coupling can become a problem. This was avoided

by increasing the distance of adjacent lines, although the total area expanded a bit.

A. High-Frequency Design Methodology

At mm-wave frequencies, the electromagnetic characteristics of the layout become significant. Accurate modeling of the parasitics becomes more important as the frequencies increase, since parasitic inductances and capacitances affect the circuit operation considerably. The designed LNA was simulated with Agilent ADS, and Momentum was used as the EM-simulator. All essential elements of the LNA, such as the transmission lines, crucial components and connections, were EM-simulated. The results were thereafter embedded into the transistor-level circuit simulations, so that the effect of the parasitics could be studied.

With the designed LNA, several electromagnetic effects had to be considered. As an example, Fig. 3 shows the connections of the cascoded transistors and the base capacitor. The signal lines at the base and collector are close enough to experience coupling, which can be taken into account with EM-simulations. Additionally, the effect of the parasitic capacitance C_{par} on the circuit performance could be considered accurately by EM-simulating the transistor connections.

Another important consideration was the parasitic inductance of the base capacitor C_{b1-2} connection to the cascode transistor base, since it implemented the base inductance L_{b1-2} . A minor variation of the L_{b1-2} value had a significant effect on the performance, so precise modeling was crucial. The LNA was simulated with the parasitics of the base capacitors and the connections to the CB-transistor bases in order to detect possible instability.

One main design issue was providing an adequate access to ground. The transmission lines needed a well defined ground for correct operation, and the shunt capacitors demanded a clear ground connection. The DC-collector currents were also large enough to require an unobstructed access to the ground. With the designed LNA, a sufficient ground for the circuit was provided by placing ground metal over the entire LNA core area.

IV. SIMULATION RESULTS

The 140-GHz LNA was designed with 130-nm SiGe BiC-MOS technology. Fig. 4 presents the final layout of the designed LNA. The finalized design has been submitted to the foundry for fabrication.

The total area of the LNA core is 320 $\mu\text{m} \times 324 \mu\text{m}$. From the core area has been omitted DC-pads and -capacitors, and RF-pads. The DC-pads are placed above and below, and the

$$H(j\omega) = - \frac{g_m r_o R_L (g_m r_o + A)}{-\omega^2 r_o^2 C_{\pi 1} R_S (C_{\pi 2} + C_{par} A) + j\omega (r_o^2 (C_{\pi 2} + C_{par} A) + C_{\pi 1} R_S (r_o (g_m r_o + 2A) - R_L (g_m r_o + A))) + r_o (g_m r_o + 2A - g_m R_L) - R_L A} \quad (3)$$

$$H(j\omega) = - \frac{g_m^2 r_o^2 R_L}{-\omega^2 r_o^2 C_{\pi 1} R_S (C_{\pi 2} + C_{par} A) + j\omega (r_o^2 (C_{\pi 2} + C_{par} A + C_{\pi 1} R_S g_m)) + r_o^2 g_m} \quad (4)$$

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER LOW-NOISE AMPLIFIERS OPERATING AT 100-200 GHz

	Technology	Frequency band (GHz)	Gain (dB)	NF (dB)	S_{11} (dB)	P_{DC} (mW)	Area (mm ²)
This Work	130-nm SiGe BiCMOS	140	18.7	7.2	-20	15	0.10
[6]	130-nm SiGe BiCMOS	108-143	20-27.5	5.5-6.5	< -7	12	0.39
[7]	130-nm SiGe BiCMOS	140	32.8	7.8	< -10	39.6	0.07
[8]	65-nm CMOS	160	13.8	7	-10	57	0.3
[9]	130-nm SiGe BiCMOS	190	24.7	9.8	< -10	21.3	0.48
[10]	130-nm SiGe BiCMOS	112-156	21-25.3	5.9	< -8	30	0.56
[11]	130-nm SiGe BiCMOS	110	20.5	4	< -10	17	0.41
[12]	28-nm FDSOI CMOS	160	15.7	8.5	< -10	32	0.34

Fig. 4. The layout of the designed LNA.

RF-pads are at the right and left sides. The effect of the RF-pad parasitics was taken into account by simulating the LNA with the parallel capacitor C_{pad} at the input and output, which value was estimated as 12 fF.

The DC-power consumption of the LNA is 15 mW with the supply voltage of 2 V and the total DC-collector current of 7.5 mA. Fig. 5 shows the simulated S-parameters and noise figure. At 140 GHz, S_{21} is 18.7 dB, which adequately meets our goal. The input and output are sufficiently matched at 140 GHz, since S_{11} and S_{22} are below -19 dB. NF of 7.2 dB is achieved at 140 GHz. The LNA stability was determined by calculating μ and μ' . Both $\mu > 1$ and $\mu' > 1$ at 1 GHz - 300 GHz, so the LNA is unconditionally stable at that frequency range. The linearity performance was analyzed by determining IIP3 and 1-dB compression point. IIP3 is -10.5 dBm, and the 1-dB compression point is -20.5 dBm. Linearity of the designed LNA is a less significant feature, since few interferers exist at 140 GHz, and the input signal power is usually weak.

V. CONCLUSION

A 140-GHz low-noise amplifier was designed with 130-nm SiGe BiCMOS technology. The LNA consists of two cascode

Fig. 5. The simulated S-parameters and noise figure of the LNA.

stages. Gain is improved with a base resonator, which design methodology was explained. The parasitic capacitance caused by the connection of the cascode transistors is minimized with dedicated layout design, so that the effect of the capacitance is negligible.

The LNA achieves gain of 18.7 dB and noise figure of 7.2 dB at 140 GHz. Both S_{11} and S_{22} are below -19 dB, so the input and output are well matched.

Table I represents a comparison of LNAs at this frequency range. As our aim was, our design stands out with a small area and low power while other metrics still remain close to state-of-the-art. The core size of the LNA is only 0.1 mm² and the power consumption is 15 mW. Therefore, it is a suitable candidate for a radiometer IC that will consist of several parallel receiver chains.

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