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Mask material effects in cryogenic deep reactive ion etching

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Cryogenic silicon etching in inductively coupled SF₆/O₂ plasma has been studied, especially the behavior of mask materials. Suitability of eight different mask materials for cryogenic silicon deep reactive ion etching has been investigated. Three of the five photoresists suffered from cracking during cryogenic etching. We clarified the stages of the etching process and identified two mechanisms behind the cracking: thermal expansion mismatch and mechanical deformation from wafer clamping and backside helium pressure. Also thickness of the photoresist plays a role in cracking, but, contrary to common conception that all thick resists suffer from cracking in cryogenic etching, we found that SU-8 negative resist did not crack, even for very thick layers. This is explained to be due to its high cross-linking density. All three hard mask materials had high selectivities and were free of cracking problems. However, aluminum mask resulted in poor surface quality, while thermally grown SiO₂ and amorphous Al₂O₃ deposited by atomic layer deposition showed smooth surfaces and sidewalls. Silicon dioxide had selectivity of 150:1, while Al₂O₃ selectivity was 66 000:1. This extreme selectivity of Al₂O₃ mask, combined with good surface quality, is shown to be highly beneficial in both shallow and through-wafer etching. © 2007 American Vacuum Society. [DOI: 10.1116/1.2734157]

I. INTRODUCTION

Cryogenic deep reactive ion etching (DRIE) of silicon was first introduced by Tachi *et al.* in 1988.¹ They observed that etch rate and selectivity increased at cryogenic temperatures but more importantly, the anisotropy of etching improved remarkably. Nowadays cryo-DRIE is commonly utilized in fabrication of microelectromechanical systems because of its ability to produce high-aspect-ratio structures at high etch rates ($>5 \mu\text{m}/\text{min}$).^{2,3} The biggest advantage of cryo-DRIE over the pulsed Bosch process⁴ is sidewall smoothness.

Selection of the etch mask material is an important issue. The etch rate of the mask must be low, but its application and patterning should be easy. The most natural mask material is photoresist, but selectivity of photoresists is usually poor compared to hard masks and therefore deep etching may not be possible with photoresist masks.⁵ In cryogenic DRIE, the other major downside of the photoresists is their vulnerability to cracking. Thin photoresists ($<1.5 \mu\text{m}$) are reported to be free of problems but thicker resists are prone to cracking.⁶ Plasma damage to resists exposed to temperatures in excess of glass transition temperature (T_g) is known to inflict problems,⁷ but photoresist cracking at cryogenic temperatures has not been given attention before. Mask material selection may also affect etch rate, undercutting,^{8–10} and surface quality of the etched features.^{8,11}

Hard masks such as silicon dioxide and metals are often utilized when high selectivity is needed.^{12,13} Hard masks are not known to be vulnerable to cracking at cryogenic temperatures. Working with hard masks adds deposition and

etching steps to the process, and, for instance, isotopic hard mask profile results in poor dimensional control.¹⁴ Deposition of the hard mask may also require high-temperature process steps. In fluorine-based plasmas, some hard mask materials such as aluminum may also inflict formation of microroughness on the etched silicon surfaces.^{8,11}

In this work, two etch processes are presented in detail and they are used to investigate suitability of five different photoresists and three different hard mask materials for cryo-DRIE. We identify two cracking mechanisms behind the photoresist cracking. We also demonstrate that $1.5 \mu\text{m}$ is not the upper limit for photoresist thickness if photoresist is chosen and prepared properly. Besides the stability of masking materials at cryogenic etching conditions, we also study the effects of masking materials on surface quality of the etched features and silicon etch rate. Al₂O₃ hard mask is compared to aluminum and silicon dioxide that have high selectivity and good surface quality, respectively.

II. EXPERIMENT

Experiments were carried out in Plasmalab System 100 reactor (Oxford Instruments). The system has two power sources: high-density SF₆/O₂ plasma is generated with inductively coupled plasma (ICP) source at 13.56 MHz and ion energies are controlled separately with capacitively coupled plasma (CCP) source also at 13.56 MHz. Mechanical clamping of the wafer and helium backside cooling ensure the effective heat exchange between the liquid nitrogen cooled electrode and the wafer.

The positive photoresists used were AZ 1505, AZ 5214 E, and AZ 4562, all products of Clariant. Both negative photoresists ma-N 415 and SU-8 50 were purchased from Micro

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TABLE I. Baking and spinning parameters for all resists and measured resist thicknesses. Baking were performed in an oven unless otherwise stated. Priming was performed in hexamethyl disilazane before spinning, except for SU-8 that was applied without any priming. HF dip was made to SU-8 wafers before prebake.

Resist	Prebake (min)	Spinning (30 s) (rpm)	Soft bake	Hard bake (min)	Thickness (μm)
AZ 1505	5	4000	20 min	30	0.5
AZ 5214E	5	4000	20 min	20–90	1.5
AZ 4562	5	4000	90 min	30–90	6.0
ma-415	5	3000	90 s ^a	...	3.0
SU-8 50	90	2500	15 min+ 10 min ^b	5–25	60

^aBaking was done on a hot plate at 95 °C.

^bBaking was done on a hot plate. First 15 min at 65 °C and then 10 min at 95 °C.

Resist Technology. Baking sequences, spinning speeds, and resulting photoresist thicknesses of all resists under investigation are presented in Table I.

Plasmlab System 400 dc magnetron sputter (Oxford Instruments) was used in static mode to sputter aluminum at room temperature. The deposition rate of aluminum was approximately 200 nm/min. Amorphous aluminum oxide was deposited by atomic layer deposition (ALD) in Thin Film Systems TFS 500 from Beneq Corp. Trimethylaluminum and water vapor were the source gases. The deposition took place at 220 °C and the deposition rate was approximately 1.05 Å/cycle. Silicon dioxide was made by standard wet oxidation in Centrotherm furnace at 1050 °C.

Standard 100 mm (100) silicon wafers were used. Test patterns had different size trenches and pillars ranging from 2 to 100 μm . The pattern loading was 50%. Surface quality of the etched features was observed using a Digiscope optical microscope and a DSM-950 scanning electron microscope (SEM), both products of Zeiss Opton. The etch depths were measured with a DEKTAK 3 profilometer from Sloan.

III. RESULTS AND DISCUSSION

A. Characterization of etch rate, profile, and process parameters

In cryogenic DRIE, temperature plays an important role. Without low stage temperatures ($T \leq (-100\text{ °C})$), it is impossible to achieve anisotropic etching results (Fig. 1). It is problematic that only the stage temperature can be controlled directly. The wafer temperature can be substantially higher. The temperature of the wafer is not dependent only on the stage temperature, but also the helium backside pressure has a big role.¹⁵

Detailed guidelines for cryoetch optimization have been given by de Boer *et al.*³ However, all processes have to be optimized because the results are influenced not only by process parameters but also by other factors such as the size and the shape of mask opening, aspect ratio of the etched features, pattern loading, and masking material.^{16,17} Parameters for two etch processes that are used to investigate the mask material effects are presented in Table II. “Base line” process results in vertical sidewalls with a reasonably high etch rate and small undercutting in “through-wafer” process the etch

rate is maximized. The sidewalls are slightly negatively tapered and undercutting pronounced because of the higher process pressure, but the etch rate is very high for cryo-DRIE process and the etched surfaces are smooth.

B. Stages of etching process and photoresist cracking

In the first experiment, the behavior of patterned photoresists at cryogenic temperatures was studied. All photoresists were patterned on 525 μm thick wafers. The wafers were loaded into the cooled process chamber, clamped, kept there for 2 min, and taken out. Neither gas flow nor rf power was applied. The temperature of the stage was -110 °C . It was

FIG. 1. Temperature dependency of the etch profiles. (a) When stage temperature is -110 °C , the etch profiles are anisotropic, (b) but when stage temperature is raised to -60 °C , etch profiles are isotropic. All other process parameters are identical.

TABLE II. Process parameters of the two optimized etching processes. In both processes, the stage temperature was -110°C , and helium backside pressure was 10 Torr for 2 min cooling period and was 5 Torr for etching, which resulted in helium leakage less than 5 SCCM during etching.

Process name	ICP power (W)	CCP power (W)	O ₂ flow (sccm)	SF ₆ flow (sccm)	Pressure (mTorr)	Loading (%)	Etch rate ($\mu\text{m}/\text{min}$)
Base line	1000	2	6	40	10	11 ^a	4.3 ^a
Through wafer	2000	3	15	100	19.5	1	7.6

^aBy decreasing the pattern loading in Base line process from 11% to 1%, nearly $5 \mu\text{m}/\text{min}$ etch rate could be achieved.

found out that AZ 4562 and ma-N 415 did not tolerate low temperatures. Both photoresists were full of small cracks after unloading. AZ 1505, AZ 5214 E, and SU-8 did not experience any problems.

In the second experiment, the wafers were loaded inside the process chamber, clamped, and 10 Torr helium backside pressure was turned on for 2 min. Stage temperature was -110°C . rf power was not applied. During the experiment, AZ 5214 E resist was damaged, which indicates that helium backside cooling may also initiate the cracking.

In the third experiment, the wafers were loaded, cooled down, and etched for 8 min using base line process. The experiment shows that the etching step after cooling is not responsible for the cracking. In our experiments, AZ 1505 and SU-8 did not suffer from cracking. If the photoresist can tolerate cryogenic temperature and helium backside cooling, it is a suitable mask for cryogenic etching. The results are summarized in Table III.

Figure 2 shows that the small resist areas between the patterns remain intact, but the large resist areas without patterns are severely damaged. It can also be observed that the cracked resist patterns are transfer into silicon during etching which is fatal to devices and therefore cracking is not just an aesthetic problem.

The effect of the cooling rate was also studied. The wafer was loaded inside the process chamber at room temperature. The stage was cooled down to -110°C for ~ 25 min. Still, AZ 5214 E cracked when helium backside pressure was turned on. Very slow cooling would also be very impractical.

TABLE III. Behavior of different photoresists during cryogenic DRIE.

Photoresist	Layer thicknesses (μm)	Cracking problems
AZ 1505	0.5	Not observed
AZ 4562	6.0	Always at low temperatures
AZ 5214 E	1.5	Sometimes when He-backside cooling is turned on
ma-N 415	2.6	Always at low temperatures
SU-8 50	7,20,60	Not observed

C. Cracking mechanisms of photoresist

Evolution of stresses in thin films has been the focus of many studies.^{18–20} Cracking of thin NiAl metal¹⁸ and poly(methylsilsequioxane) polymer¹⁹ films during cooling part of thermal cycling has been reported. Thermal stresses induced by the thermal expansion mismatch between the thin film material and the silicon substrate cause wafer deformation as depicted in Fig. 3. Small defects in thin films can easily create pinholes and cracks under tensile stress.²¹ The numerical values of the coefficients of thermal expansion (CTE) are presented in Table IV. Stresses built up during thermal cycling in the thinner films have been reported to be somewhat higher than stresses in thicker films.^{18,19} Still, be-

(a)

(b)

FIG. 2. Photoresist cracking. Optical microscope and SEM pictures of the test structures patterned with AZ 5214 E photoresist. Both pictures were taken after etching.

FIG. 3. Thin film tensile stress and mechanical deformation induced by mismatch of thermal expansion. Separate silicon substrate and photoresist (a) at room temperature and (b) at -110°C . (c) Substrate and photoresist together at -110°C .

cause of better stress tolerance of thinner films, only thick films are prone to cracking. This is consistent with the general observation that thin resist photoresist masks are more suitable for cryo-DRIE. Because of the thermal stresses, also AZ 4562 and ma-N 415 photoresist layers were damaged when brought into contact with liquid nitrogen cooled electrode. The film cracking relaxes the stresses.

The clamping of the wafer and the high pressure difference between the two sides of the wafer inflict wafer deformation like the one depicted in Fig. 4. The maximum deformation of a circular wafer under pressure is given by

$$h = \left(\frac{r^4 \Delta p (1 - \nu)}{2.67 E t} \right)^{1/3},$$

where r is the radius of the wafer, Δp the pressure difference between the two sides of the wafer, ν the Poisson's ratio of silicon, t the thickness of the wafer, and E the Young's modulus of silicon.²² The radius of the wafers is 50 mm, the Young's modulus of (100) silicon is 130 GPa, and the Poisson's ratio is 0.27. The backside pressure of the wafer is 10 Torr and the pressure inside the process chamber is 10 mTorr. The deformations calculated for three different

TABLE IV. CTEs for different materials. CTE of AZ 1350 can be used as an approximation for all AZ resists.

Material	Coefficient of thermal expansion (ppm/ $^{\circ}\text{C}$)
Silicon	2.6
SU-8	52
AZ 1350	100
SiO ₂	0.5
Aluminum	23
Al ₂ O ₃	8.1

FIG. 4. Tensile stress and wafer deformation caused by helium backside pressure. The pressure above the wafer is 10 mTorr, and during cooling period the backside pressure is 10 Torr.

wafer thicknesses according the equation above are presented in Table V. The calculated values are in good agreement with the deformations measured by Aachboun *et al.*²³ The deformation of the wafer induces new stresses into the photoresist which is already under the stress caused by the CTE mismatch. To clarify if the wafer deformation caused by the cooling system plays a role in photoresist cracking, 1.5 μm thick AZ 5214 E photoresist layer was patterned on three wafers with different thicknesses of 250, 525, and 1000 μm .

The wafers were loaded into the cooled process chamber, clamped and 10 Torr helium backside pressure was applied. The photoresist on the 1 mm thick wafer did not crack. This is believed to be because of the mechanical strength of the 1 mm thick wafer. The resist on 525 μm thick wafer cracked during the experiment because of the greater wafer deformation. The measurement using 250 μm thick wafer failed. The helium leakage to the chamber during the experiment was over 60 standard cubic centimetres per minute (sccm), which indicates that the sealing between the process chamber and the helium cooling system was extremely poor. The resist on the 250 μm thick wafer was intact after experiment, but the pressure difference between the cooling system and the process chamber was not 10 Torr as in previous experiments because of the helium leakage. Therefore the last result is not comparable.

The results presented in Table V strongly suggest that the wafer deformation caused by the helium backside cooling also plays a role in photoresist cracking at low temperatures. It must be emphasized that wafer deformation caused by helium cooling system by itself is not enough to cause photoresist cracking, but it is evidently one mechanism that can initiate cracking at cryogenic temperatures. It was also noticed that AZ 5214 E photoresist cracks easier if the etching is done immediately after lithography, which is probably because of larger temperature gradient.

D. Stability of SU-8

The base material of most positive photoresists is Novolac resin [see Fig. 5(a)].²⁴ Because of the chemical construction of the resin, the polymer chains in positive photoresists are linear and are therefore mechanically not very strong. The base material of the negative SU-8 photoresist is EPON SU-8 resin, which has eight functional epoxy groups in one

TABLE V. Effect of wafer deformation induced by the cooling system on cracking of AZ 5214 E photoresist.

Wafer thicknesses (μm)	Calculated wafer deformation (μm)	Observations
1000	260	No problems during processing
525	320	Sometimes problems when He cooling is turned on
250	410 ^a	No proper sealing between helium cooling and chamber

^aBecause of the poor sealing between the helium cooling system and the chamber, the real deflection is substantially smaller than the calculated one.

molecule [see Fig. 5(b)]. Therefore the cross-linking density of SU-8 is exceptionally high and the mechanical strength is good.²⁵ This is believed to be the reason why SU-8 layers at least up to 60 μm are resistant to cracking during cryogenic etching. The CTE of SU-8 is also better matched to substrate properties than the CTE of AZ resists (see Table IV).

To make sure that the high cross-linking density is the reason why SU-8 does not crack, 60 μm thick SU-8 layers were patterned on two 1 mm thick wafers. All spinning and baking parameters were identical and they are presented in Table I. Only the postbake times were varied because the postbake time affects on the cross-linking density of SU-8.

The post bake time of the first wafer was 25 min while the second wafer was baked only for 5 min. Both wafers were loaded into the cooled process chamber, kept there for 3 min, and etched for 2 min and 30 s using base line process and unloaded. The highly cross-linked (25 min bake) SU-8 layer did not experience any problems during the experiment, while the mildly cross-linked (5 min bake) SU-8 layer was full of cracks and adhesion between the wafer and the SU-8 layer also failed. The result suggests that the high cross-linking density is the factor why SU-8 does not crack during cryogenic etching.

E. Photoresist selection criteria

When using AZ 1505 photoresist mask, all etched surfaces are smooth, but low selectivity and thin mask layer thickness limit its use to shallow etchings. Thicker AZ photoresist layers are prone to cracking. In our experiments, the only thick photoresist that did not crack at cryogenic temperatures was SU-8. Therefore selectivity does not limit the etch depth, but troublesome removal of SU-8 narrows down the practical applications of SU-8 as an etch mask. Surface quality of etched silicon is good when using SU-8 mask (Fig. 6) if mask layer is not extremely thick. Sidewall roughness might become a problem when using 60 μm thick SU-8 mask.

F. Hard masks: SiO_2 , Al, and Al_2O_3

Three different hard mask materials were patterned on 525 μm thick silicon wafers. Buffered hydrofluoric acid

FIG. 5. (a) Basic structure of Novolac resin. (b) Average structure of EPON SU-8.

FIG. 6. Trenches etched using 7 μm thick SU-8 mask. Etched surfaces are smooth if SU-8 layer is not extremely thick.

TABLE VI. Measured etch depths after 8 min etching step and resist removal. No significant catalytic effects of aluminum mask could be observed.

Mask material	Etch depth (μm)	Etch rate ($\mu\text{m}/\text{min}$)
SiO_2	19.2	2.40
Al	20.4	2.55
Al_2O_3	19.7	2.46
AZ 5214 E	19.7	2.46

(BHF) solution that was heated up to 32°C was used to etch $1.40\text{ }\mu\text{m}$ thick thermal SiO_2 layer. Aluminum and Al_2O_3 films of 200 and 48 nm, respectively, were etched in Al-etch PS 70-10 solution from Merck. The temperature of the solution was 50°C . Silicon was etched using base line process.

In our experiments, none of the three hard mask materials suffered from cracking during the 3 min long cooling period and the 8 min long etching step because of the better matching of CTEs and better mechanical properties (see Table IV). The average etch depths, measured using profilometer, and the calculated etch rates are presented in Table VI. Also the etch depth reached with AZ 5214 E mask is included. All etched depths are within 6%. Highest etch depth is measured when using aluminum mask. Fedynyshyn *et al.*^{8,9} reported that aluminum mask generates catalytic reactions, and therefore the etch rate is significantly higher when using Al mask. Later a few groups have reported pronounced undercutting when using aluminum mask.^{10,26}

In our experiments, the silicon etch rate was slightly higher when using Al mask. This difference is believed to be within normal wafer-to-wafer reproducibility in a single wafer DRIE equipment rather than caused by catalytic reactions. However, if aluminum generates catalytic reactions, they probably enhance silicon etch rate only in the vicinity of the mask and therefore in deep etchings the effect is insignificant.

G. Surface quality and selectivity

Surface quality of the etched features was clearly affected by the mask material choice as can be seen from Fig. 7.

Aluminum is known to have extremely high selectivity against silicon in fluorine-based plasmas,⁵ but it may also initiate formation of silicon “grass” on bottom of the etched trenches.^{8,27} In our experiments, redeposition of the aluminum led to micromasking, and under highly anisotropic etching conditions, silicon grass was formed. Sintering the aluminum at 450°C for 30 min before etching reduced the grass formation but did not eliminate it. Because of the grass formation, the usefulness of the aluminum as a mask material is limited mainly to through-wafer etching applications. We demonstrated etching of vias through a $380\text{ }\mu\text{m}$ thick wafer with a 200 nm aluminum mask with average etch rate above $7\text{ }\mu\text{m}/\text{min}$ using through-wafer process. This shows that cryo-DRIE can compete with Bosch process also in very deep etching applications.²⁸

(a)

(b)

FIG. 7. Effect of masking material on quality of etched surfaces. (a) Aluminum mask initiates formation of grass, (b) but when using Al_2O_3 mask all the etched surfaces are smooth.

Silicon dioxide is a commonly used mask material in DRIE of silicon,¹² because the growth and the deposition of SiO_2 are easy, its selectivity is high (150:1) compared to photoresist masks, and patterning can be done selectively in BHF or by RIE. Also the quality of the etched surfaces is excellent when utilizing a SiO_2 mask.

Amorphous Al_2O_3 is a much less studied mask material.^{29,30} In our experiments, Al_2O_3 mask did not have negative impact on the surface quality of etched silicon. The selectivity of Al_2O_3 against silicon is reported to be 32 in pure SF_6 inductively coupled plasma.²⁹ We demonstrated etching through a $400\text{ }\mu\text{m}$ thick wafer using a 6 nm thick Al_2O_3 mask, which translates to selectivity of 66 000:1. Another significant advantage of the aluminum oxide mask over thermal oxide is its considerably lower deposition temperature (220°C). Compared with plasma enhanced chemical vapor deposited silicon dioxide, Al_2O_3 has much better step coverage. Combination of fairly low deposition temperature, fully conformal deposition profile, high selectivity, and good etched surface quality makes Al_2O_3 very attractive mask material. Aluminum oxide can also be easily patterned by phosphoric acid based wet etchants.

IV. CONCLUSIONS

The behavior of the eight different mask materials during cryogenic DRIE was studied. Three of the five photoresists used suffered from cracking. AZ 1505 and SU-8 of any thickness were not vulnerable to cracking in our experi-

ments. Thin resists are known to be suitable for cryogenic etching,⁶ but remarkable result was that SU-8 layers at least up to 60 μm were also suitable for cryogenic processing. The experimental results suggest this to be due to the exceptionally high cross-linking density of SU-8.

It was demonstrated that there are two cracking mechanisms: besides thermal expansion mismatch stresses, also the mechanical wafer deformation induced by the helium back-side cooling system has an important role in the cracking mechanism of photoresists at cryogenic temperatures. The cracking risk decreases when using a mechanically strong thick substrate. Still a hard mask should be utilized whenever it is possible because none of the hard masks under investigation showed cracking problems.

Thin photoresists can be used only in shallow etchings because of their relatively poor selectivity. Hard masks are needed in deep etchings. Silicon dioxide is a common and reliable mask material, but its selectivity is only moderate. Aluminum has extremely high selectivity and it is easy to pattern, but because of the micromasking phenomenon, its use is limited to through-wafer etching. Amorphous aluminum oxide mask deposited by ALD combines all good properties of silicon dioxide and aluminum. It has extremely high selectivity, low deposition temperature, fully conformal deposition profile, and the quality of etched surfaces is good. These properties make aluminum oxide a very promising masking material for both shallow and through-wafer DRIE processes.

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