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Study of Cu-Sn-In system for low temperature, wafer level solid liquid inter-diffusion bonding

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Abstract— *The Solid Liquid Interdiffusion (SLID) bonds carried out for this work take advantage of the Cu-In-Sn ternary system to achieve low temperature wafer-level bonds. The experiments were carried out across a range of temperatures and the results cover optimized wafer-level bonding process, the formation of the bond microstructure, mechanical performance, as well as the effects of thermal aging.*

Keywords—copper, tin, indium

I. INTRODUCTION

The rapid growth of Internet of Things (IoT) and Cyber Physical Systems (CPS) and their role in the Trillion Sensor Vision bring requirements for additional verticality in 3D packaging as well as increased diversity in cap wafer materials. This type of highly miniaturized packaging requires a comprehensive understanding of residual stresses incurred during processing. Solid Liquid Interdiffusion bonding (SLID) has been identified as a solution to realize these more complex 3D packages while also allowing for hermetic sealing, required for Micro-Electromechanical Systems (MEMS) structures. [1, 3].

Successful SLID bonds utilizing the Cu-Sn system have been carried out at temperatures close to 300°C [4-10]. Additionally, several other binary material systems like, Ag-In [11-13], Au-In [14-16], Cu-In [17], Ag-Sn [18, 19], Ni-Sn [20, 21] and Au-Sn [22-29] have also been demonstrated potential for SLID bonding. However, reducing the bonding temperatures to below 250°C results in reduced residual stresses caused by mismatch in the thermal expansion locally between Cu and Si or globally between other cap materials (such as germanium, glass or sapphire). A novel Low Temperature Cu-In-Sn wafer-level SLID bond is carried out in this work by leveraging the 110°C eutectic melting point between Sn and In. The resulting inter-metallic compounds created in these bonds maintains a high re-melt temperature to ensure that the bonds do not re-melt during subsequent higher temperature processes [2].

II. METHODS AND MATERIALS

A. Wafer Preparation

Each bonding experiment was carried out using two 4" double side polished (DSP) Si wafers with a <100> crystal orientation. The backsides of the wafers were patterned using a standard lithography process and the Si was etched using reactive ion etching (RIE). A 30nm TiW barrier/adhesion layer followed by a Cu seed-layer of 150 nm was sputtered on the frontside of all wafers. The pattern of the lithography mask, the bond features and the alignment marks are shown in fig. 1. A standard lithography process was utilized for the patterning of micro-bumps with dimensions ranging from 10µm x 10µm up to 250µm x 250µm. The experiments were then carried out in two separate paths using two different material stacks and bonding equipment. The photoresist was stripped, and the field metallization layers were etched by means of wet chemistry.

Fig. 1 bonding features and alignment marks

B. Aalto Bonding Experiments

The experiments completed in Aalto University utilized a symmetrical material stack demonstrated in Fig. 2. A targeted thickness of 4µm Copper was electrochemically deposited, followed by a desired layer thickness 2µm Sn and 2µm In on both wafers. The electroplated features were measured after each step with a DektakXT contact profilometer. The results

of the profilometry showed that on average $4.3 \pm 0.3 \mu\text{m}$ Cu, $2.3 \pm 0.2 \mu\text{m}$ Sn and $1.3 \pm 0.3 \mu\text{m}$ In were present across the

Fig. 2 bonding features and alignment marks

wafer. Low temperature bonding experiments were conducted using different bonding temperatures (200°C and 250°C) for a fixed time of 1hr and a fixed pressure of 18MPa. Wafers are placed into the AML-AWB-04 wafer bonder and roughly aligned at ambient temperature and pressure. The bonding chamber is evacuated and then preheated to 75°C before carrying out fine alignment. Contact is made after alignment and then the desired bonding pressure of 18MPa is applied. A controlled heating of cycle of 20°C/s is initiated until the desired bonding temperature is reached. The wafers are held at the target bonding temperature and pressure for the duration of the hour-long bonding time. After the bonding time has expired the heaters are switched off and the bonding pressure is released. The wafers are allowed to cool for approximately one hour until they reach a temperature of 150°C before venting the bonding chamber and removing the bonded wafer pair. Dicing of the bonded wafers was conducted using a Disco DAD3220 dicing saw. A selection of diced chips was molded and prepared for cross section analysis and a range of the remaining chips were thermally aged at 150° for 500 hours and their tensile strength was tested using the MTS 858 system. Fracture surfaces and cross-sections were then analyzed using optical microscopy as well as with JSM-6330F field emission Scanning Electron Microscope (SEM) which is equipped with Energy-Dispersive X-ray Spectroscopy (EDS).

C. EV Group Bonding Experiments

In bonding experiments carried out by the EV Group the cap wafer was processed identically to the Aalto experiments, however the carrier wafer was plated with 4μm Cu only. In order to manage the native Cu-Oxide, the device wafers (i.e. the wafers without Sn and In plating) were pre-treated with diluted citric acid. One wafer was additionally cleaned using organic solvents (prior to citric acid treatment) in order to remove possible organic residues. The wafers were aligned face-to-face on EVG SmartView® NT2 semi-automated wafer to wafer aligner and subsequently bonded on an EVG520IS semi-automated wafer bonder. The bonding recipe was translated to the EV Group wafer bonder in order to repeat same bonding process conditions which were used during Aalto Bonding Experiments. The bonded wafers were analyzed by scanning acoustic microscopy using a PVA Tepla SAM 450.

III. RESULTS

All bonds were carried out in the absence of 10μm features due to the lithography process having been optimized for larger 250μm feature sizes. The 10μm features

are present after development of the photo resist and electrochemical deposition of the material stack. However, during the resist stripping and field metallization etching processes, the smallest features were damaged as seen in Fig. 3.

Fig. 3 Optical micrographs of damaged features and alignment marks features.

A. Aalto Bonding Results

Successful bonds were carried out in Aalto University. However, even though alignment accuracy in the AML-AWB-04 wafer bonder is 1μm, it has not been reliably achievable. It has been shown experimentally that the alignment achieved in the AML-AWB-04 used for these experiments is upwards of 5μm and as such insufficient for the bonding of smaller feature sizes (10μm, 25μm).

Fig. 4 demonstrates a SEM cross section of successful Cu-In-Sn SLID bonds carried out at both 200°C and 250°C with information regarding their elemental analysis. The resultant bonds show minimal voiding and no residual Sn or In indicating that all the low melting point material has reacted. The results of the EDS for the 200°C bond showed two distinct intermetallic phases, a Cu rich $\text{Cu}_3(\text{Sn},\text{In})$ near the Cu-Sn interfaces and $\text{Cu}_6(\text{Sn},\text{In})_5$ in the center of the bond. The 250°C sample reveals a bond that is comprised of mostly $\text{Cu}_3(\text{Sn},\text{In})$ with some locations at the center of the bond being comprised of $\text{Cu}_6(\text{Sn},\text{In})_5$.

The formation of the interconnection microstructure during bonding can be rationalized by utilizing the isothermal sections from Cu-In-Sn ternary system [add ref]. As can be seen from Fig. 5 when Cu starts to dissolve into liquid phase

Fig. 4 SEM cross sections of successful bonds carried out at 200°C (top) and 250°C (bottom).

having about 65at-% Sn (estimated based on the original Sn to In thickness ratio) the liquid phase becomes supersaturated with Cu and in local equilibrium with $\text{Cu}_6(\text{Sn,In})_5$. As indicated by the direction of tie lines the In|Sn ratio in $\text{Cu}_6(\text{Sn,In})_5$ should be slightly higher than the initial ratio. As also shown by the isothermal section $\text{Cu}_6(\text{Sn,In})_5$ can't be in local equilibrium directly with Cu and therefore either $\text{Cu}_3(\text{Sn,In})$ or CuIn_Delta phase should nucleate between $\text{Cu}_6(\text{Sn,In})_5$ and Cu.

Fig. 5 Isothermal section at 250C from ternary Cu-In-Sn system.

As expected, based on the original In|Sn thickness ratio, the presence of $\text{Cu}_3(\text{Sn,In})$ was confirmed with EDS measurements. Additionally, due to the mass balance requirement, the In|Sn ratio in $\text{Cu}_3(\text{Sn,In})$ should be clearly lower than in $\text{Cu}_6(\text{Sn,In})_5$. After the formation of the initial diffusion path $\text{Cu}|\text{Cu}_3(\text{Sn,In})|\text{Cu}_6(\text{Sn,In})_5|\text{Liq}$ the local nominal composition (LNC) starts to change. Based on the mass balance it is known that the LNC must follow the contact line (shown with the dashed line in Fig. 5). As can be seen from the micrographs in Fig. 5 the liquid phase has been consumed during the bonding and, therefore, the local nominal Cu content is $> 55\text{at-\%}$ indicating that the re-melting temperature of the bond has increased up to $\sim 600^\circ\text{C}$.

Samples were annealed at 150°C for 504hrs and the results are pictured in Fig 6. SEM cross section and EDS analysis reveals that both bonds demonstrate good stability as the phases of both bonds remained unchanged.

Fig. 6 SEM cross sections of 200°C (top) and 250°C (bottom) bonded samples that have been thermally aged at 150° for 504 hours.

It is interesting to note that In drastically stabilizes the microstructure in comparison to binary Cu-Sn system. As can be seen from Fig. 6 there is still clearly $\text{Cu}_6(\text{Sn,In})_5$ phase visible between the $\text{Cu}_3(\text{Sn,In})$ layers even after 504 hours annealing at 150°C . Based on the available assessed thermodynamic data it can be shown that the dissolved indium stabilizes $\text{Cu}_6(\text{Sn,In})_5$ phase much more than $\text{Cu}_3(\text{Sn,In})$ phase. When calculating the Gibbs energy for the formation of the phases with the estimated In content the ΔG_f increase for $\text{Cu}_6(\text{Sn,In})_5$ is almost 50% (from -7150 J/mol up to -10600 J/mol) and for $\text{Cu}_3(\text{Sn,In})$ the ΔG_f increase is only $\sim 6\%$ (from -8300 J/mol to -8830 J/mol). Therefore, the driving force for Cu through $\text{Cu}_3(\text{Sn,In})$ that is required for further microstructural evolution is significantly reduced.

Fig. 7 Tensile failure mode schematic.

In tensile tests a minimum of 24MPa tensile strength was recorded. Fracture surfaces of the tested samples were analyzed by optical microscopy and showed that practically all fractures were adhesion failures propagating Si|TiW or TiW|Cu interface as pictured in Fig. 7. This indicates that the bonds were stronger than their adhesion to Si.

B. EV Group Bonding Results

The 250°C bonded wafers showed overall good quality as can be observed from the acoustic microscope images shown in Fig 8. It is to be noted that some unbonded features can be observed (highlighted in red). Those correlate with the missing Cu features on the device wafer. Based on the C-SAM inspection the alignment accuracy was $\sim 5\mu\text{m}$ in both x- and y-directions

Fig 8. C-SAM images from wafers bonded at 250°C

The bond quality of the wafers that were bonded at 200°C was observed to be much worse and majority of the chips detached during the dicing phase. The problems were most probably due to the combined effect of poor wetting caused by Cu oxidation and damaged or missing Cu features from the wafer manufacturing process.

As can be seen from Fig. 9 the bond microstructures are similar to those observed from Aalto bonds. However, since there were Sn and In only on one wafer the amount of liquid is half of that found in Aalto bonds and therefore the $\text{Cu}_6(\text{Sn},\text{In})_5$ phase can be observed only at the bond periphery (squeeze out) area.

Fig 9. SEM Cross section of 250°C bond with asymmetrical material stack showing the $25\mu\text{m}$ bonds

IV. CONCLUSION

Low temperature wafer level SLID bonds were successfully fabricated down to 200°C. The resultant bonds showed minimal voiding and defects. The addition of indium to a traditional Cu-Sn system appears to significantly stabilize the $\text{Cu}_6(\text{Sn},\text{In})_5$ phase. Tensile strength tests demonstrated that the Cu-In-Sn bonds outperformed the under-bump metallization. Further experiments should be carried out to characterize the mechanical properties of the indium containing intermetallic phases. Additionally, process related optimizations such as lithography optimization for smaller micro-bumps and optimizing a stable process to bond asymmetrical materials stacks are required. Unfortunately, full use of EVG's advanced wafer bonding capabilities could not be fully utilized due to issues related to the test wafer processing.

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REFERENCES

- [1] M. Tilli, M. Paulasto-Krockel, M. Petzold, H. Theuss T. Motooka, and V. Lindroos, Handbook of Silicon Based MEMS Materials and Technologies, 3rd ed. Elsevier, 2020
- [2] A. Lis, S. Kicin, F. Brem, and C. Leinenbach. Thermal Stress Assessment for Transient Liquid-Phase Bonded Si Chips in High-Power Modules Using Experimental and Numerical Methods. *Journal of Electronic Materials*, 46(2):729–741, Feb. 2017.
- [3] Liu, X.J. *et al.* "Experimental determination and thermodynamic calculation of the phase equilibria in the Cu-Sin-Sn system." *Journal of Electronic Materials*, pp.1093-1103. (2001)
- [4] H. Xu, T. Suni, V. Vuorinen, J. Li, H. Heikkinen, P. Monnoyer, and M. Paulasto-Kröckel. Wafer-level SLID bonding for MEMS encapsulation. *Advances in Manufacturing*, 1(3):226– 235, Sept. 2013. K. Elissa, "Title of paper if known," unpublished.
- [5] A. Duan, K. Wang, K. E. Aasmundtveit, and N. Hoivik, "Reducing the bond frame width in Cu/Sn SLID wafer level packaging," 2012 4th Electron. Syst. Technol. Conf. ESTC 2012, 2012.
- [6] A. Hilton and D. S. Temple, Wafer-Level Vacuum Packaging of Smart Sensors, vol. 16, no. 11. 2016
- [7] P. Ramm, J. Ji-Q. Lu, and M. M. V. Taklo, Handbook of Wafer Bonding. Wiley, 2012
- [8] . Brincker, S. Söhl, R. Eisele, and V. N. Popok, "Microelectronics Reliability Strength and reliability of low temperature transient liquid phase bonded Cu \ \ Sn \ \ Cu interconnects," *Microelectron. Reliab.*, vol. 76–77, pp. 378–382, 2017
- [9] C. T. Ko and K. N. Chen, "Wafer-level bonding/stacking technology for 3D integration," *Microelectron. Reliab.*, vol. 50, no. 4, pp. 481–488, 2010.
- [10] H. Liu, G. Salomonsen, K. Wang, K. E. Aasmundtveit, and N. Hoivik, "Wafer-level Cu/Sn to Cu/Sn SLID-bonded interconnects with increased strength," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 1, no. 9, pp. 1350–1358, 2011.
- [11] T. T. Luu, A. Duan, K. E. Aasmundtveit, and N. Hoivik, "Optimized Cu-Sn wafer-level bonding using intermetallic phase characterization," *J. Electron. Mater.*, vol. 42, no. 12, pp. 3582–3592, 2013.

- [12] W. P. Lin, C. Sha, and C. C. Lee, "40 μm Flip-Chip Process Using Ag – In Transient Liquid Phase Reaction," *Packag. (Boston, Mass.)*, vol. 2, no. 6, 2012.
- [13] C. Lee, A. Yu, L. Yan, H. Wang, J. H. He, Q. X. Zhang, and J. H. Lau, "Characterization of intermediate In/Ag layers of low temperature fluxless solder based wafer bonding for MEMS packaging," *Sensors Actuators, A Phys.*, vol. 154, no. 1, pp. 85–91, 2009.
- [14] J. C. Lin, L. W. Huang, G. Y. Jang, and S. L. Lee, "Solid-liquid interdiffusion bonding between In-coated silver thick films," *Thin Solid Films*, vol. 410, no. 1–2, pp. 212–221, 2002.
- [15] B. J. Grummel, Z. J. Shen, H. A. Mustain, and A. R. Hefner, "Thermo-mechanical characterization of au-in transient liquid phase bonding die-attach," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 3, no. 5, pp. 716–723, 2013.
- [16] V. Chidambaram, C. Bangtao, G. C. Lip, and D. Rhee Min Woo, "Au-in-based hermetic sealing for MEMS packaging for down-hole application," *J. Electron. Mater.*, vol. 43, no. 7, pp. 2498–2509, 2014.
- [17] L. Deillon, A. Hessler-Wyser, T. Hessler, and M. Rappaz, "Solid-liquid interdiffusion (SLID) bonding in the Au–In system: experimental study and 1D modelling," *J. Micromechanics Microengineering*, vol. 25, no. 12, p. 125016, 2015.
- [18] Y.-C. Chen and C. C. Lee, "Indium-copper multilayer composites for fluxless oxidation-free bonding," *Thin Solid Films*, vol. 283, no. 1–2, pp. 243–246, 1996.
- [19] Q. Guo, F. Yu, H. Chen, and M. Li, "Microstructure evolution during reflow and thermal aging in a Ag@Sn TLP bondline for high-temperature power devices," *J. Mater. Sci. Mater. Electron.*, vol. 29, no. 4, pp. 3014–3024, 2018.
- [20] J. F. Li, P. A. Agyakwa, and C. M. Johnson, "Kinetics of Ag₃Sn growth in Ag-Sn-Ag system during transient liquid phase soldering process," *Acta Mater.*, vol. 58, no. 9, pp. 3429–3443, 2010.
- [21] S. W. Yoon, M. D. Glover, and K. Shiozaki, "Nickel-tin transient liquid phase bonding toward high-temperature operational power electronics in electrified vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2448–2456, 2013.
- [22] H. P. R. Frederikse, R. J. Fields, and A. Feldman, "Thermal and electrical properties of copper-tin and nickel-tin intermetallics," *J. Appl. Phys.*, vol. 72, no. 7, pp. 2879–2882, 1992.
- [23] T. Suni, H. Xu, V. Vuorinen, H. Heikkinen, S. Vahanen, A. Jaakkola, P. Monnoyer, and M. Paulasto-Krockel, "Wafer-level AuSn and CuSn bonding for MEMS encapsulation," *Microelectron. ...Microelectronics Packag. Conf.*, pp. 1–5, 2013.
- [24] T. A. Tollefsen, A. Larsson, O. M. Lövvik, and K. Aasmundtveit, "Au-sn SLID bonding - Properties and possibilities," *Metall. Mater. Trans. B Process Metall. Mater. Process. Sci.*, vol. 43, no. 2, pp. 397–405, 2012.
- [25] H. Xu, A. Rautiainen, V. Vuorinen, E. Österlund, T. Suni, H. Heikkinen, P. Monnoyer, and M. Paulasto-Kröckel, "Reliability performance of Au-Sn and Cu-Sn wafer level SLID bonds for MEMS," in *Proceedings of the 5th Electronics System-Integration Technology Conference, ESTC 2014*, 2014.
- [26] H. Xu, T. Suni, V. Vuorinen, J. Li, H. Heikkinen, P. Monnoyer, and M. Paulasto-Kröckel, "Wafer-level SLID bonding for MEMS encapsulation," *Adv. Manuf.*, vol. 1, no. 3, pp. 226–235, 2013.
- [27] K. E. Aasmundtveit, T. T. Luu, H. V. Nguyen, R. Johannessen, N. Hoivik, and K. Wang, "Au-Sn fluxless SLID bonding: Effect of bonding temperature for stability at high temperature, above 400°C," *Electron. Syst. Integr. Technol. Conf. ESTC 2010 - Proc.*, pp. 0–5, 2010.
- [28] S. Marauska, M. Claus, T. Lisec, and B. Wagner, "Low temperature transient liquid phase bonding of Au/Sn and Cu/Sn electroplated material systems for MEMS wafer-level packaging," *Microsyst. Technol.*, vol. 19, no. 8, pp. 1119–1130, 2013.
- [29] T. A. Tollefsen, O. M. Lövvik, K. Aasmundtveit, and A. Larsson, "Effect of temperature on the die shear strength of a Au-Sn SLID bond," *Metall. Mater. Trans. A Phys. Metall. Mater. Sci.*, vol. 44, no. 7, pp. 2914–2916, 2013.
- [30] A. Larsson, T. Andre, K. Høydalsvik, D. A. G. W. Breiby, and K. Aasmundtveit, "Au-Sn SLID Bonding : A Reliable HT Interconnect and Die Attach Technology," 2013.