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Modeling of Multiport DC Busses in Power-Electronic Systems

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***Abstract*—This paper deals with dynamic modeling of multiport DC busses, which are increasingly applied in various DC-power distribution systems, such as hybrid powertrains and DC microgrids. Parasitic impedances of long DC cabling together with distributed DC capacitors introduce a potential risk of small-signal instabilities in the DC bus, if resonance frequencies of the bus appear below (or around) switching frequencies of power-electronic converters. In order to predict the resonance behavior of the bus, a systematic approach for dynamic modeling of the DC bus in power-electronic systems is presented. The DC-bus model is validated by means of experiments. Furthermore, application of the model in small-signal analysis and time-domain simulations is illustrated.**

***Index Terms*—Cable, DC bus, modeling, multiport.**

I. Introduction

Multiport DC busses are applied in emerging applications, such as industrial and household DC distribution systems [1], more-electric aircraft [2], powertrains of electrified transportation systems [3], and non-road mobile machineries [4]. An example of a system with a multiport DC bus is shown in Fig. 1. In these kind of applications, the DC bus is typically distributed, i.e., DC capacitors are placed inside individual converters, which may be located far away from each other. Therefore, parasitic DC-cable impedances become considerable, and they have to be taken into account in the control design and system stability assessments. Furthermore, the change of the capacitor type from electrolytic capacitors to film capacitors introduces a need to examine the system stability with decreasing capacitance values.

The risk of instability in a cascade-connected system consisting of a DC source, an LC filter, and a regulated load is well known. The stability analysis and design methods have been considered for regulated DC loads [5]–[8] as well as for three-phase AC loads [9]–[15]. Traditionally, nonlinear models of regulated DC or AC loads have been first averaged over the switching cycle and then linearized for small-signal analysis purposes. The small-signal stability has been studied by means of linearized models, which are typically expressed in a form of state-space representations or transfer functions. The product of the source impedance and the load admittance (called as a minor loop gain) together with the Nyquist criterion have been used to analyze the small-signal stability, cf. [6], [7] and references therein. Alternatively, the local stability has been analyzed based on the eigenvalues of the linearized system, e.g. [3]. Typically, constant-power loads have been assumed, leading to a negative conductance as a small-signal model. In more advanced load admittance models, the effect of nonideal control loops has been considered [13], [14]. Furthermore, the sampling and pulse-width modulator (PWM) delays have been taken into account in [12], [15].

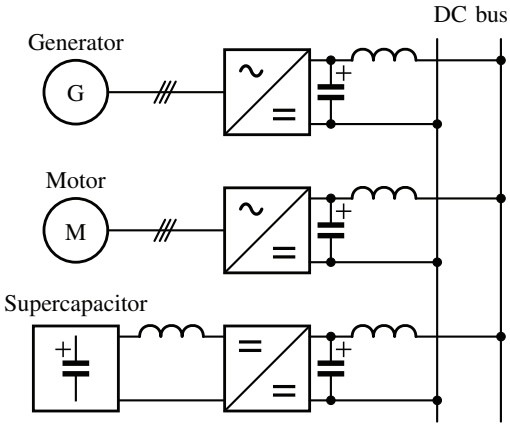


Fig. 1. Example system equipped with a DC bus, where parasitic cable inductances are also shown. This system could be, e.g., a hybrid powertrain of a mobile working machine or a future building equipped with a DC distribution network. Naturally, the system could include more sources, loads, and energy storages.

Recently, the above mentioned concepts have been applied to developing stabilizing controllers for systems involving multiport DC busses [2], [8], [16], while systematic derivation of multiple-input-multiple-output (MIMO) models for the DC bus has mostly been disregarded. As the number of ports increases, developing state-space equations or transfer functions becomes laborious without a systematic approach. Furthermore, increase in the number of the ports adds resonance frequencies to the bus. Moreover, these resonances appear typically in the range of 1…20-kHz frequency. Therefore, it is important to take the phase-shifting effect of the delays properly into account on load admittance modeling.

Contributions of this paper are on the systematic multiport DC-bus modeling approach, presented in Section II. The proposed modeling approach is experimentally validated in Section III-A. An application example in Section III-B illustrates the risk of instability in the DC bus by means of small-signal analysis and time-domain simulations.

II. Modeling of a DC Bus

The DC-bus impedance is considered to consist of the input capacitances of power-electronics converters and DC cabling

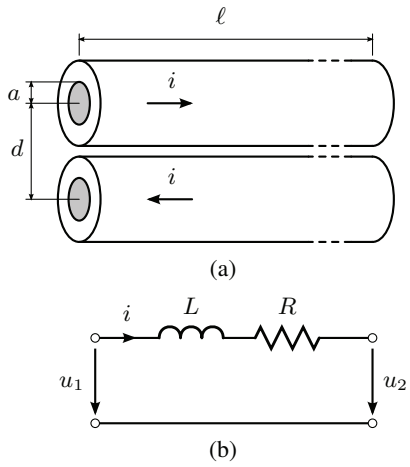


Fig. 2. DC transmission line: (a) dimensions; (b) model.

between them. The converters with their loads are modeled as admittances, which are connected to ports of the DC bus.

A. Cabling

Fig. 2(a) illustrates dimensions of a DC transmission line. The corresponding equivalent circuit is shown in Fig. 2(b)[1]. The DC values for the cable inductances and resistances are considered. These low-frequency values can be seen to yield a worst-case scenario from the point of resonances, since the inductances are overestimated and resistances are underestimated compared to their values at high frequencies.

The self-inductance of the transmission line at low frequencies may be estimated with [17]

$$L = \frac{\mu_0 \ell}{\pi}\left[\ln\left(\frac{d}{a}\right) + \frac{1}{4}\right] \tag{1}$$

where ℓ is the length of the transmission line, a is the conductor radius, d is distance between the cable centers, and $\mu_0 = 4\pi \cdot 10^{-7}$ H/m is the permeability of free space. The first term inside the brackets corresponds to the external inductance and the second term corresponds to the internal inductance. The internal inductance decreases with the frequency due to the skin effect. As an example, the ratio $d/a = 5$ yields $L/\ell =$ 0.74 μH/m.

The DC resistance of the transmission line is

$$R = \frac{2\ell}{\sigma A} \tag{2}$$

where $A = \pi a^2$ is the cross section of the wire, and σ is the conductivity ($\sigma = 5.8 \cdot 10^7$ S/m for copper). The resistance increases significantly with the frequency due to the skin effect and temperature. Furthermore, the real cabling parameters differ from (1) and (2), e.g., due to uncertainties in the actual dimensions. However, these fundamental equations can be used as a starting point, if measurement data is not available.

[1]In this paper, a voltage arrow from positive towards negative is used to represent polarity.

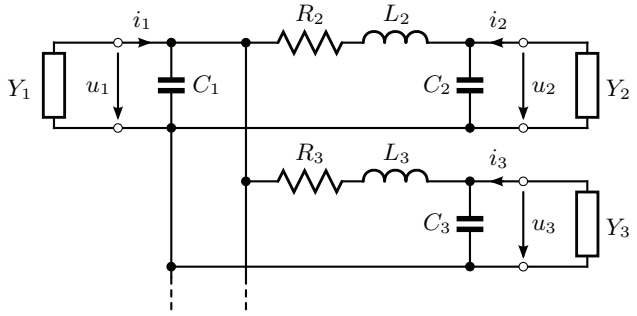


Fig. 3. DC-bus model. Admittances $Y_1 \dots Y_n$ represent load (and source) models, which can be, e.g., nonlinear time-domain models or small-signal transfer functions.

B. Capacitors

DC capacitors are typically located inside the power-electronic converters. However, from the modeling point of view, it is more convenient to include them as a part of the DC-bus model. A DC capacitor could be modeled in a wide range of frequencies as

$$Z_{\mathrm{C}}(s) = \frac{1}{sC} + sL_{\mathrm{C}} + R_{\mathrm{C}} \tag{3}$$

where C is the capacitance, L_{C} is the equivalent series inductance, and R_{C} is the equivalent series resistance of the capacitor. The undamped natural frequency

$$\omega_0 = \frac{1}{\sqrt{L_{\mathrm{C}} C}} \tag{4}$$

corresponding to the impedance in (3) is typically higher than switching frequencies applied in DC-power distribution systems. Hence, ideal DC capacitors will be assumed in the DC-bus model. In order to increase the frequency range of the DC-bus model, the equivalent series inductances of the capacitors could be taken into account.

C. Dynamic DC-Bus Model

Fig. 3 shows a DC-bus model (augmented with load models). Without loss of generality, the inductance between port 1 and the point of common coupling is zero. The inductors model the parasitic inductance of long cables. Due to the capacitors connected across each port, the inputs of the system are the currents $i_1 \dots i_n$ and the outputs are the capacitor voltages $u_1 \dots u_n$.

First, the DC bus with three ports is considered for simplicity. Based on Fig. 3, the state equations can be written as

$$C_1 \frac{\mathrm{d}u_1}{\mathrm{d}t} = i_1 + i_{\mathrm{L2}} + i_{\mathrm{L3}} \tag{5a}$$

$$C_2 \frac{\mathrm{d}u_2}{\mathrm{d}t} = i_2 - i_{\mathrm{L2}} \tag{5b}$$

$$C_3 \frac{\mathrm{d}u_3}{\mathrm{d}t} = i_3 - i_{\mathrm{L3}} \tag{5c}$$

$$L_2 \frac{\mathrm{d}i_{\mathrm{L2}}}{\mathrm{d}t} = u_2 - u_1 - R_2 i_{\mathrm{L2}} \tag{5d}$$

$$L_3 \frac{\mathrm{d}i_{\mathrm{L3}}}{\mathrm{d}t} = u_3 - u_1 - R_3 i_{\mathrm{L3}} \tag{5e}$$

where i_{L2} and i_{L3} refer to inductor currents. If n ports are assumed, the state equations can be expressed in matrix form as

$$\boldsymbol{C}\frac{\mathrm{d}\boldsymbol{u}}{\mathrm{d}t} = -\boldsymbol{F}\boldsymbol{i}_{\mathrm{L}} + \boldsymbol{i} \tag{6a}$$

$$\boldsymbol{L}\frac{\mathrm{d}\boldsymbol{i}_{\mathrm{L}}}{\mathrm{d}t} = \boldsymbol{G}\boldsymbol{u} - \boldsymbol{R}\boldsymbol{i}_{\mathrm{L}} \tag{6b}$$

where the input current vector is $\boldsymbol{i} = [i_1, i_2, \cdots, i_n]^{\mathrm{T}}$ and the voltage vector is $\boldsymbol{u} = [u_1, u_2, \cdots, u_n]^{\mathrm{T}}$. The capacitance matrix is

$$\boldsymbol{C} = \begin{bmatrix} C_1 & 0 & \cdots & 0 \\ 0 & C_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & C_n \end{bmatrix} \tag{7}$$

and inductance and resistance matrices are

$$\boldsymbol{L} = \begin{bmatrix} L_2 & 0 & \cdots & 0 \\ 0 & L_3 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & L_n \end{bmatrix} \quad \boldsymbol{R} = \begin{bmatrix} R_2 & 0 & \cdots & 0 \\ 0 & R_3 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & R_n \end{bmatrix} \tag{8}$$

The coupling matrices $\boldsymbol{F}$ and $\boldsymbol{G}$ are

$$\boldsymbol{F} = \begin{bmatrix} -1 & -1 & \cdots & -1 \\ 1 & 0 & \cdots & 0 \\ 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 1 \end{bmatrix} \quad \boldsymbol{G} = \begin{bmatrix} -1 & 1 & 0 & \cdots & 0 \\ -1 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ -1 & 0 & 0 & \cdots & 1 \end{bmatrix} \tag{9}$$

Other kind of couplings could be modeled in a similar way.

Based on (6), the port voltages can be expressed as

$$\begin{aligned} \boldsymbol{u}(s) &= [s\boldsymbol{C} + \boldsymbol{F}(s\boldsymbol{L} + \boldsymbol{R})^{-1}\boldsymbol{G}]^{-1}\boldsymbol{i}(s) \\ &= \boldsymbol{Z}(s)\boldsymbol{i}(s) \end{aligned} \tag{10}$$

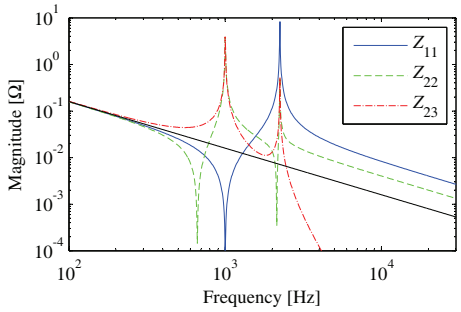
where $\boldsymbol{Z}(s)$ is the impedance matrix. If the resistance $\boldsymbol{R} = \boldsymbol{0}$ is assumed, the resonance frequencies of $\boldsymbol{Z}(s)$ can be solved from

$$\det(\omega^2\boldsymbol{I} - \boldsymbol{C}^{-1}\boldsymbol{F}\boldsymbol{L}^{-1}\boldsymbol{G}) = 0 \tag{11}$$

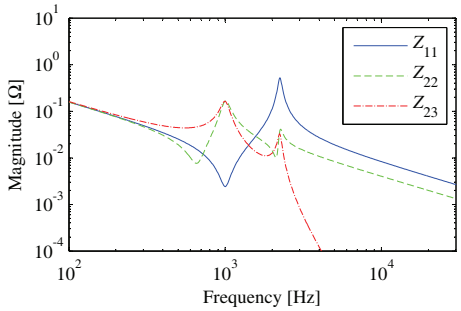
A three-port DC bus is considered as an example. Hence, the representation in (10) reduces to

$$\begin{bmatrix} u_1(s) \\ u_2(s) \\ u_3(s) \end{bmatrix} = \begin{bmatrix} Z_{11}(s) & Z_{12}(s) & Z_{13}(s) \\ Z_{12}(s) & Z_{22}(s) & Z_{23}(s) \\ Z_{13}(s) & Z_{23}(s) & Z_{33}(s) \end{bmatrix} \begin{bmatrix} i_1(s) \\ i_2(s) \\ i_3(s) \end{bmatrix} \tag{12}$$

In order to illustrate the resonances and antiresonances, the impedances $|Z_{11}(\mathrm{j}\omega)|$, $|Z_{22}(\mathrm{j}\omega)|$, and $|Z_{23}(\mathrm{j}\omega)|$ of a lossless DC bus are first shown in Fig. 4(a). Resonance frequencies calculated using (11) are 1.0 kHz and 2.24 kHz. For comparison, Fig. 4(a) also shows the impedance of the stiff system. Fig. 4(b) shows impedances with realistic resistances based on (2). As expected, the resonance frequencies are almost equal to the lossless case.



(a)



(b)

Fig. 4. Impedances: (a) lossless DC bus ($R_2 = R_3 = 0$) and the stiff system ($L_2 = L_3 = 0$); (b) DC bus with realistic resistances. Capacitances are $C_1 = 2$ mF and $C_2 = C_3 = 4$ mF and inductances are $L_2 = L_3 = 6.3$ μH.

D. Loads and Sources

In Fig. 3, admittances $Y_1 \ldots Y_n$ represent load and source models. Since the same concepts hold for modeling both loads and sources, the term load is used in the following. The load model can be, e.g., a detailed nonlinear model, as illustrated in Fig. 5(a). However, conclusions based on only nonlinear time-domain models may be difficult to draw. Thus, the small-signal behavior in the vicinity of an operating point can be described by means of a linearized small-signal model, such as the admittance shown in Fig. 5(b). These methods together give a tool for analyzing and illustrating the stability margin of the system. Some aspects of small-signal modeling are briefly discussed in the following.

In order to derive a small-signal model, the original nonlinear model is first averaged over a switching period. The resulting switching-cycle averaged model is valid up to around the switching frequency if two samples per switching cycle are taken. A well-defined switching-cycle averaged model can be expressed as a nonlinear state-space representation, which can be unambiguously linearized by means of well-known techniques. The system to be linearized can be complicated since control loops and their delays should be taken into account. However, more insight into the system can be obtained with the help of linearized models as compared to using time-domain simulations or experiments only. Linearized input admittances of three-phase converters have been considered in, e.g., [14], [15], [18].

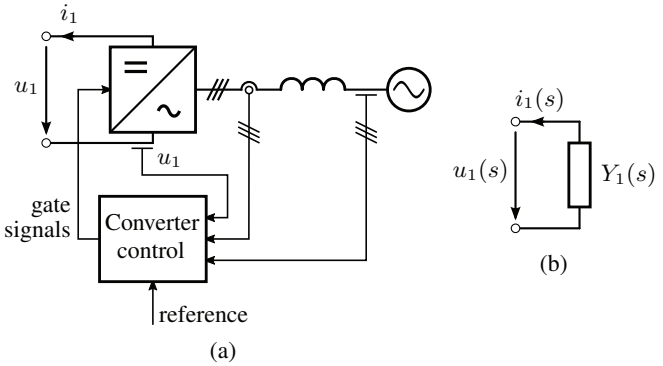


Fig. 5. Example three-phase load model: (a) block diagram of nonlinear system; (b) linearized small-signal model.

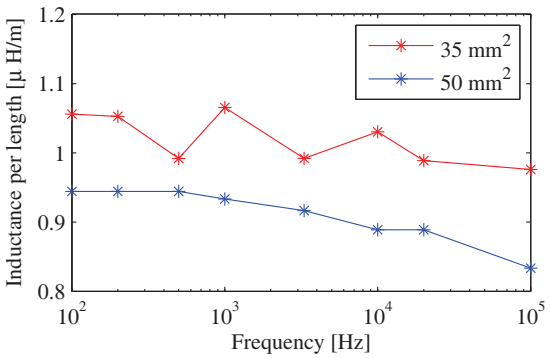


Fig. 6. Measured inductance of 35-mm^2 and 50-mm^2 DC cables. Measurements were performed with an RLC meter.

As a result of the linearizing procedure, the transfer function $Y_1(s) = -i_1(s)/u_1(s)$ can be obtained in the case of the example system shown in Fig. 5, where the sign of the current flowing to the load is defined in accordance with Fig. 3. Using matrix notation, the load current vector $\boldsymbol{i}(s)$, which is the input of the DC bus model, can be expressed as

$$\boldsymbol{i}(s) = -\boldsymbol{Y}(s)\boldsymbol{u}(s) \tag{13}$$

In the case of a distributed control of each load, the admittance matrix is

$$\boldsymbol{Y}(s) = \begin{bmatrix} Y_1(s) & 0 & \cdots & 0 \\ 0 & Y_2(s) & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & Y_n(s) \end{bmatrix} \tag{14}$$

Furthermore, the load model could be augmented with external disturbances [such as a varying AC-side voltage in Fig. 5(a)] with Norton or Thevenin equivalent sources. Without any external inputs, the closed-loop system consisting of the DC-bus model and load admittances becomes

$$[\boldsymbol{I} + \boldsymbol{Z}(s)\boldsymbol{Y}(s)]\,\boldsymbol{u}(s) = \boldsymbol{0} \tag{15}$$

If delays are included in the linearized model, it is convenient to apply the loop gain matrix $\boldsymbol{Z}(s)\boldsymbol{Y}(s)$ (whose elements are the minor loop gains) and open-loop analysis methods such as the Nyquist and Bode plots, when studying the stability and robustness of the system.

III. Results

A. Experimental Validation of the DC Bus Model

Typical cable dimensions in (1) and (2) with the minimum distance d between cable centers (obtained from cable datasheets) yield the inductance range of $0.8\ldots0.35$ μH/m and the resistance range of $23\ldots0.11$ mΩ/m with the cross section range of $1.5\ldots300$ mm^2, respectively. In practice, the distance d is larger than its minimum value calculated from datasheets, which increases the actual inductance. Fig. 6 shows inductances of 35-mm^2 and 50-mm^2 DC cables measured using an RLC meter. Hereafter, the value of $L/\ell = 1$ μH/m will be used.

TABLE I
DC-Bus Parameters Corresponding to Fig. 7

$C_1 = C_2 = C_3$ [μF]	L_2 [μH]	L_3 [μH]	R_2 [mΩ]	R_3 [mΩ]
360	3.4	3.7	3.3	3.6

In order to validate the DC-bus model presented in Section II-C, impedances of a three-port DC bus were measured using a frequency response analyzer. The schematic of the DC bus is illustrated in Fig. 3. The DC transmission lines were composed of 35-mm^2 cables, and their lengths were $\ell_2 = 3.4$ m and $\ell_3 = 3.7$ m. Resulting parameters are given in Table I.

The measured and modeled impedances $Z_{11}(\mathrm{j}\omega)$ are shown in Fig. 7. It can be seen that the measured impedance agrees very well with the model up to frequencies of 15 kHz. At higher frequencies, the series inductance $L_\mathrm{C} = 60$ nH of the capacitors affects: the measured phase begins to turn as inductive (towards $+90°$) and the antiresonance corresponding to (4) occurs at the frequency of 36 kHz. Minor differences between the measured and modeled impedances below frequencies of 15 kHz are mainly due to the skin effect.

B. Application Example

1) Example System: The block diagram of the example system is shown in Fig. 8. This system has three ports: a vector-controlled grid-connected converter is connected to port 1, an open-loop controlled induction motor drive to port 2, and port 3 is open. In both converters, a space-vector PWM is used, and the duty ratios are calculated based on the measured DC-bus voltages. Discretized controllers with sampling period of $T_\mathrm{s} = 1/(2f_\mathrm{sw})$ are used, where f_sw is the switching frequency, and sampling is synchronized to the PWM. The total delay in the discrete control systems is $T_\mathrm{d} = (3/2)T_\mathrm{s}$, which consists of the computation delay (T_s) and sample-and-hold behavior of the PWM ($T_\mathrm{s}/2$). The parameters of the example system are given in Table II.

The voltage controller calculates the reference power as

$$P_\mathrm{ref} = \frac{C_1}{2}\left(k_\mathrm{p} + \frac{k_\mathrm{i}}{s}\right)\left(u_\mathrm{1,ref}^2 - u_1^2\right) \tag{16}$$

where C_1 is the capacitance of the grid-connected converter,

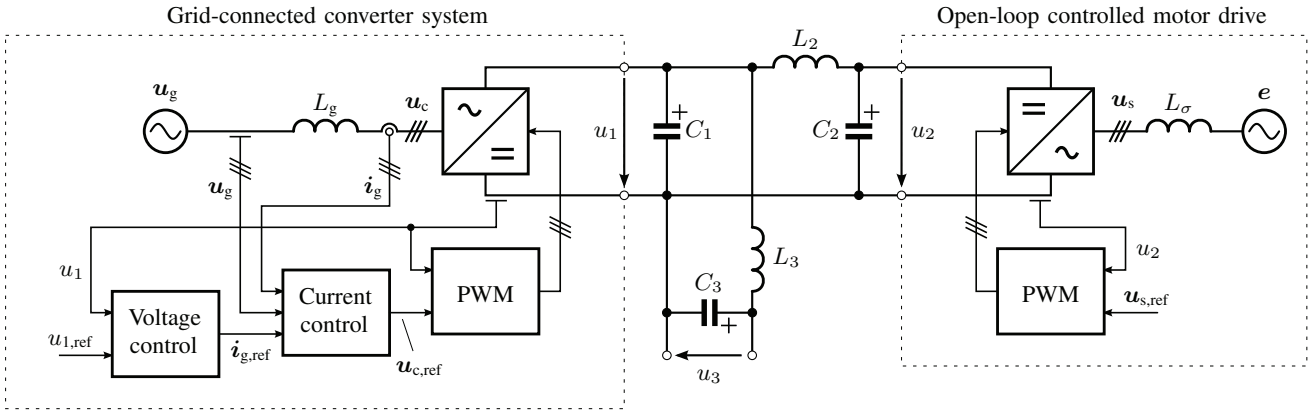


Fig. 8. Example system consisting of a vector-controlled grid-connected converter in port 1, an open-loop controlled induction motor drive in port 2, and port 3 is open. Resistors in series with inductors are not shown in the figure.

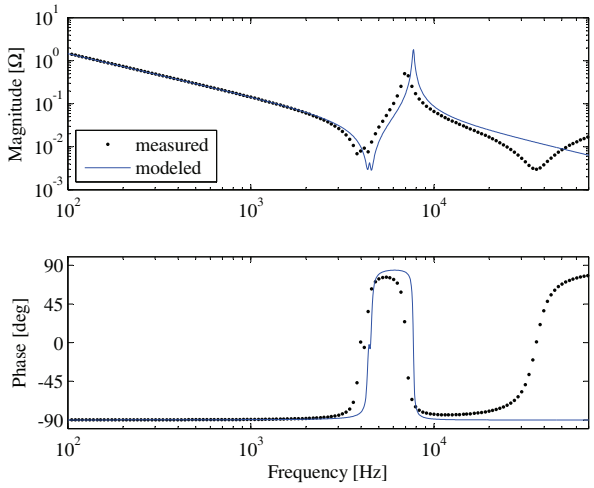


Fig. 7. Measured and modeled frequency responses of the impedance $Z_{11}(\mathrm{j}\omega)$. Parameters given in Table I were used in the model.

and the gains are $k_\mathrm{p} = 2\zeta\omega_\mathrm{n}$ and $k_\mathrm{i} = \omega_\mathrm{n}^2$.[2] The reference grid current in grid-voltage coordinates is obtained as

$$\boldsymbol{i}_{\mathrm{g,ref}} = \begin{bmatrix} i_{\mathrm{gd,ref}} \\ i_{\mathrm{gq,ref}} \end{bmatrix} = \begin{bmatrix} \frac{2}{3}\frac{P_\mathrm{ref}}{\|\boldsymbol{u}_\mathrm{g}\|} \\ 0 \end{bmatrix} \tag{17}$$

where the reactive current component $i_{\mathrm{gq,ref}}$ is set to zero. A PI-type current controller in synchronous coordinates is applied in the grid-connected converter [19].

The open-loop controlled motor drive is modeled as a three-phase LR load and the back emf. The parameters of the load correspond to a 160-kW induction motor [18].

2) Small-Signal Analysis: The load models of the example system were linearized in a similar way to [15]. The delay T_d of the actual discrete-time control system was taken into account as $\exp(-sT_\mathrm{d})$. In order to determine the operating point, the AC loads were transformed to synchronous coordinates. The linearized load models were formulated as load admittances, and small-signal stability analysis of the example system was carried out in various operating points and system parameters. Since the delay is included in the model, the stability margin was evaluated by means of the loop-gain matrix $\boldsymbol{Z}(s)\boldsymbol{Y}(s)$.

As an example, Fig. 9 shows the DC-bus impedance $Z_{11}(\mathrm{j}\omega)$, the load admittance $Y_1(\mathrm{j}\omega)$, and the minor loop gain $Z_{11}(\mathrm{j}\omega)Y_1(\mathrm{j}\omega)$. The operating point and the parameters are given in Table II. The transmission-line lengths are 30 m. Based on the minor loop gain, it can be concluded that the system is unstable since the phase margin becomes 0° at around the frequency of 1 kHz while the magnitude is over 1.

[2]If inner control loops were ideal, ω_n and ζ would equal the undamped natural frequency and the damping ratio of the closed-loop transfer function from the reference DC-bus voltage to the actual DC-bus voltage.

TABLE II
PARAMETERS AND OPERATING POINT OF THE EXAMPLE SYSTEM (PHASE QUANTITIES, PEAK VALUES)

Parameter	Value
Motor drive	
Back emf $\|\boldsymbol{e}\|$	251 V
Leakage inductance L_σ	0.70 mH
Resistance R_σ	32 mΩ
Stator angular frequency ω_s	$2\pi \cdot 50$ rad/s
Power into the stator	196 kW
Switching frequency f_sw	4 kHz
Grid-connected converter system	
Voltage $\|\boldsymbol{u}_\mathrm{g}\|$	376 V
Inductance L_g	1.0 mH
Resistance R_g	4.0 mΩ
Angular frequency ω_g	$2\pi \cdot 50$ rad/s
Voltage controller	
Undamped natural frequency ω_n	$2\pi \cdot 20$ rad/s
Damping ratio ζ	1
Current controller bandwidth	$2\pi \cdot 400$ rad/s
Switching frequency f_sw	4 kHz
DC bus	
Capacitance C_1	2 mF
Capacitances $C_2 = C_3$	4 mF
Lengths of transmission lines	
Stable case: $\ell_2 = \ell_3$	5 m
Unstable case: $\ell_2 = \ell_3$	30 m
Inductance per length L/ℓ	1.0 μH/m
Resistance per length R/ℓ	0.29 mΩ/m

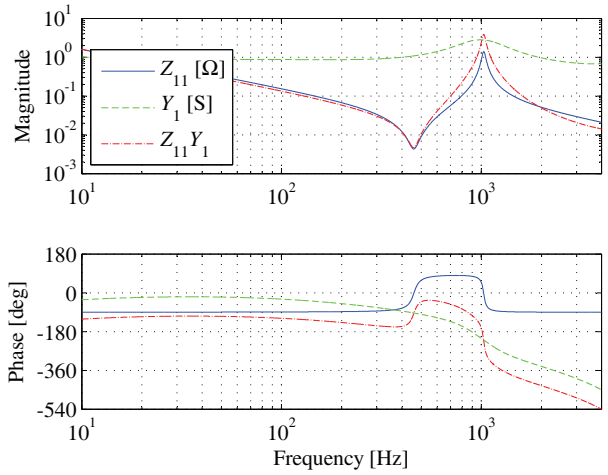


Fig. 9. Frequency responses $Z_{11}(\mathrm{j}\omega)$, $Y_1(\mathrm{j}\omega)$, and the minor loop gain $Z_{11}(\mathrm{j}\omega) \cdot Y_1(\mathrm{j}\omega)$.

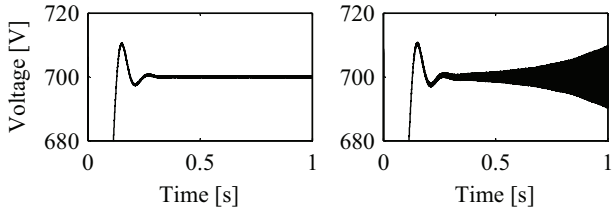


Fig. 10. Initial transient in the DC-bus voltage u_1 with 5-m (stable) and 30-m (unstable) transmission-line lengths.

Based on the linearized model, the minor loop gain at port 1 becomes stable, if the transmission-line lengths are decreased. In addition, if the direction of the power flow is reversed or the switching frequency (which determines the delay T_d) is increased, this minor loop gain also becomes stable. However, the switching frequency needs to be increased significantly, in this case up to 30 kHz. Naturally, the voltage controller gains affect the stability via load admittances, and thus, those should be chosen in accordance with the presented small-signal analysis.

3) Time-Domain Simulations: Fig. 10 shows time-domain simulation examples with parameters given in Table II. When the lengths of the transmission lines are 5 m, the system is stable. The transmission-line lengths of 30 m lead to unstable operation, seen as oscillations in the voltage u_1. Thus, the time-domain simulation results agree well with the small-signal analysis.

IV. Conclusion

A systematic modeling approach for a multiport DC busses in power-electronic converter systems is proposed. The model is valid up to resonance frequencies of the DC-bus capacitors. The model can be applied both in time-domain simulations and small-signal analysis. If the DC-bus model is augmented with load admittances, the stability margins of the system can be evaluated.

Acknowledgment

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