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A 6-Phase Two-Stage Blocker-Tolerant Harmonic-Rejection Receiver

Faizan Ul Haq, *Student Member, IEEE*, Mikko Englund, Yury Antonov, *Member, IEEE*, Miikka Tenhunen, Kari Stadius, *Member, IEEE*, Marko Kosunen, *Member, IEEE*, Kim B. Östman, Kimmo Koli, *Member, IEEE*, Jussi Ryynänen, *Senior member, IEEE*

Abstract—Modern wideband receivers need to operate linearly in the presence of strong out-of-band blockers. In this paper, we introduce a blocker tolerant harmonic rejection receiver which is able to suppress blockers at the local oscillator harmonics. The suppression is achieved by applying harmonic rejection in two stages, such that the first harmonic rejection already occurs at the first gain stage output. The proposed receiver achieves this harmonic rejection with simple 6-phase local-oscillator (LO) clocking. The proposed design also uses simple gain coefficients of ± 1 while implementing harmonic rejection in two stages compensates for the mismatch effects of each stage. In addition, near-band blocker linearity is improved by implementing a 3rd-order baseband feedback response which acts in conjunction with N-path filtering. Implemented in a 28 nm FDSOI process, the receiver demonstrates 18-37 dB harmonic rejection from the first stage and 46-53 dB of harmonic rejection in total. Further, a blocker compression point of 2.5 dBm for a third harmonic blocker and a near-band blocker compression point of -6.5 dBm is achieved.

Index Terms—Blocker resilience, Direct down conversion receivers, N-path filtering, Harmonic rejection.

I. INTRODUCTION

THE advent of multiple communication standards in recent years has created a demand for digital intensive wideband receivers. Such a receiver should be digitally tunable at a particular reception band/standard while at the same time operating in the presence of strong out-of-band blockers. Traditionally, these out-of-band blockers have mostly been attenuated through external pre-filters implemented with either surface acoustic wave or bulk acoustic wave technologies [1], [2]. However, they are bulky and cannot be tuned to cover wide frequency ranges. This means that multiple pre-filters are needed to cover various communication standards situated across a wide range of frequencies. In order to alleviate the requirement of pre-select filtering, the integrated circuit must assume a greater role in the filtering and in general blocker tolerance.

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F. Ul Haq and Y. Antonov were with Department of Electronics and Nanoengineering, Aalto University, Finland and now are with CoreHW Oy, Finland (email:faizan.ulhaq@aalto.fi)

M. Tenhunen, K. Stadius, M. Kosunen and J. Ryynänen are with Department of Electronics and Nanoengineering, Aalto University, 00076 Aalto, Finland (email:faizan.ulhaq@aalto.fi)

K. B. Östman is with Nordic Semiconductor, Finland

M. Englund and K.Koli are with Huawei Finland.

Fig. 1. a) Basic N-path filtering technique with its frequency response. b-c) Conceptual representation of 8-phase harmonic rejection N-path filtering. Weighted charging of N-path capacitors results in effective clock frequency with reduced harmonic content.

One such widely studied integrated filtering technique is N-path filtering, first presented in 60's [3] and rediscovered in recent decade [4]–[8]. Theoretically, N-path filtering can have any number of parallel paths. However, due to simplicity one of the widely implemented topologies is 4-phase N-path filtering [9]. One of this topology's shortcomings is its inability to sufficiently suppress blockers at harmonics of the local-oscillator (LO) frequency. To solve this problem, various works [8], [10]–[15] have proposed harmonic rejecting N-path filtering by utilizing more clock phases and precise weighting coefficients.

Fig. 1(b) presents a conceptual representation of a prior art 8-phase harmonic rejection N-path filtering [10], [11], [14]–[16]. In this configuration, the steady state voltages across the capacitors are weighted with multiplication factors of ± 1 and $\pm\sqrt{2}$ to create an equivalent effective clock waveform

resembling a sine wave, i.e., with reduced harmonic content. Fourier analysis of such an effective clock shows complete rejection of third and fifth harmonic. However, harmonic rejection in this architecture is achieved at the expense of a higher number of combination paths which inevitably leads to a complicated design with increased area and power consumption. In addition, harmonic rejection is usually implemented later in the receiver chain when gain has already been applied [10], [11], [16]. This means that any blocker present at the harmonics of the local-oscillator frequency (f_{LO}) will already saturate the first stages of a receiver before the harmonic rejection is applied.

Some recent works have tried to solve the above problems of harmonic rejection N-path filtering architectures. A 6-phase architecture was proposed in [17] as a radio-frequency (RF) front-end and in [8] as a standalone filter. The 6-phase architecture simplifies the LO generation as only six LO phases are required for harmonic rejection. In addition, one less mixer and baseband amplifier are needed compared to a eight-phase architecture further simplifying the design. Another work [18] simplifies the LO generation by proposing overlapping clocks with 25% duty-cycle, which are easier to generate than 12.5% duty-cycle in a eight-phase architecture. Although [17] and [18] address the problem of LO generation complexity, they do not address the second problem of blockers at LO harmonics saturating the first receiver stages.

To address the second problem, [14] and [13] have proposed harmonic rejection at the output of the first gain stage. The benefit of these techniques is that they achieve promising linearity improvements for blockers at LO harmonics. However, they still implement a higher number of N-paths and require difficult to implement gain coefficients.

In this paper, we propose a two-stage harmonic rejection radio-frequency (RF) receiver where the first stage provides harmonic rejection already at the output of the first gain stage. This helps to improve receiver linearity for blockers at LO harmonics. The proposed architecture combines the benefits of 6-phase LO clocking in [8], [17] and achieving HR at the output of first gain stage in [13], [14]. In addition, the proposed architecture only requires simple (± 1) gain coefficients, and implementing harmonic rejection in two stages compensates for the mismatch effects of each stage. We have also designed a 3rd-order filter stage in conjunction with the N-path filter, which significantly improves near-band filtering compared to traditional first-order filtering. The proposed work was first presented in [19] with the RF front-end measurements. This paper extends the [19] with additional receiver measurements, theoretical analysis, design guidelines, mismatch simulations, a new LO generation circuitry, a new feed-forward N-path phase/frequency tuning stage, and the circuit implementation details.

The organization of this paper is as follows: Section II details the conceptual description of our proposed architecture while the Section III discusses how near-band blocker rejection is achieved in the proposed design. Then in Section IV, the details of implemented HR received prototype are presented. The paper concludes with the measured results from the fabricated prototype in Section V and a conclusion in Section

VI.

II. PROPOSED HARMONIC REJECTION ARCHITECTURE

The single-ended equivalent block diagram of the proposed two-stage harmonic-rejection architecture is presented in Fig. 2. The architecture implements harmonic rejection through a 6-phase LO and three baseband downconversion paths each of which is 60° degrees phase shifted from the adjacent path. This simplifies the LO generation as only 6 LO phases are required compared to the 8-phase architecture. At first glance it may seem that the complexity of having 3 baseband paths, 3 ADCs, etc is more than 8-phase architecture. However, the increase in baseband chains from 2 to 3 brings additional benefits of 2nd stage HR which is not there in typical 8-phase architecture. The addition of 2nd HR compensates for mismatches in the system. Further, the proposed 6-phase architecture utilizes simple ± 1 multipliers to generate the HR compared to 8-phase architecture.

A. First Stage of Harmonic Rejection

The first stage of harmonic rejection rejection is implemented by two parallel low-noise amplifiers (LNA) together with six differential passive mixers clocked by non-overlapping LO phases. The need for two LNA's and six mixers arises from creating harmonic rejection without overlapping LO clocks that would decrease the LNA gain. The LO clocking for the passive mixers is presented in Fig. 2. The operation of the first harmonic rejection stage can be explained as follows: During LO phases $1p$ and $2p$, $LNA1$ and $LNA2$ are connected to $BB1$ alternatively, whereas in phase $3p$ and $3n$ neither $LNA1$ nor $LNA2$ are connected to $BB1$. Finally, in phases $1n$ and $2n$ $LNA1$ and $LNA2$ are connected to $BB1$ with opposite polarity. This type of switching results in the effective LO waveform at the input of $BB1$ as shown in Fig. 2:

$$f(t+nT) = \begin{cases} 1, & 0 < t < \frac{T_{LO}}{6} \\ 1 & \frac{T_{LO}}{6} < t < \frac{T_{LO}}{3} \\ 0 & \frac{T_{LO}}{3} < t < \frac{T_{LO}}{2} \\ -1 & \frac{T_{LO}}{2} < t < \frac{2T_{LO}}{3} \\ -1 & \frac{2T_{LO}}{3} < t < \frac{5T_{LO}}{6} \\ 0 & \frac{5T_{LO}}{6} < t < T_{LO} \end{cases} \quad (1)$$

Fourier coefficients of the resulting effective LO can be calculated as:

$$a_n = \frac{1}{n\pi} \left[\sin\left(\frac{2\pi n}{3}\right) - \sin\left(\frac{5\pi n}{3}\right) + \sin(\pi n) \right] \quad (2)$$

$$b_n = \frac{1}{n\pi} \left[-\cos\left(\frac{2\pi n}{3}\right) + 1 + \cos\left(\frac{5\pi n}{3}\right) - \cos(\pi n) \right] \quad (3)$$

where n is an integer number. Based on these Fourier coefficients, the magnitude of each harmonic component is plotted in Fig. 3. One can observe no 3rd-order harmonic component in the effective LO. In reality, however, complete elimination of the third harmonic is not possible due to device mismatches and LO non-idealities. This can also be observed from the measured results in Section VI. Therefore, a second

Fig. 2. Simplified block diagram of the proposed harmonic rejection receiver.

Fig. 3. (Upper) Effective LO waveform at first stage of harmonic rejection and (lower) gain of its frequency content from Fourier analysis.

stage is employed to enhance the harmonic rejection further in a practical implementation.

B. Second Stage of Harmonic Rejection

The second stage makes the effective baseband signals more closely resemble a sine wave. To do this, we implement cross-

coupled baseband stages between three baseband paths as shown in Fig. 2. The down-converted signals V_A , V_B and V_C at the output nodes of the first baseband amplifiers are arithmetically manipulated to generate signals $(V_A - V_C)/2$, $(V_B + V_A)/2$ and $(V_C + V_B)/2$. The generated signals more closely resemble a sine wave with the normalized multiplication factors of 1, 0.5, -0.5, -1, -0.5 and 0.5. Fourier analysis of such a waveform results in:

$$f(t+nT) = \begin{cases} 1, & 0 < t < \frac{T_{LO}}{6} \\ 0.5, & \frac{T_{LO}}{6} < t < \frac{T_{LO}}{3} \\ -0.5, & \frac{T_{LO}}{3} < t < \frac{T_{LO}}{2} \\ -1, & \frac{T_{LO}}{2} < t < \frac{2T_{LO}}{3} \\ -0.5, & \frac{2T_{LO}}{3} < t < \frac{5T_{LO}}{6} \\ 0.5, & \frac{5T_{LO}}{6} < t < T_{LO} \end{cases} \quad (4)$$

$$a_n = \frac{1}{2n\pi} [\sin(\pi n) + \sin(2\pi n) + \sin(\frac{\pi n}{3}) + 2\sin(\frac{2\pi n}{3}) - \sin(\frac{4\pi n}{3}) - 2\sin(\frac{5\pi n}{3})] \quad (5)$$

$$b_n = \frac{1}{2n\pi} [\cos(2\pi n) - \cos(\frac{\pi n}{3}) - 2\cos(\frac{2\pi n}{3}) + 2\cos(\frac{5\pi n}{3})] \quad (6)$$

Based on these Fourier coefficients, the magnitude of each harmonic is plotted in Fig. 4. Ideally, one can observe no 3rd-order harmonic in the effective LO.

Fig. 4. (Upper) Effective LO waveform at second stage of harmonic rejection and (Lower) gain of its frequency contents from Fourier analysis.

Fig. 5. Simulated effect of LNA gain mismatch on the first stage of harmonic rejection.

C. Mismatch Effects

Implementing harmonic rejection in two stages has an effect of compensating for mismatch effects of each stage. To analyze these effects, Fig. 5 and 6, we observe the effect of two main mismatch sources on harmonic rejection through behavioral simulations. In Fig. 5, the effect two LNA's gain mismatch on first stage harmonic rejection is plotted. As can be observed, a 2% variation in LNA relative gain already reduces the harmonic rejection from 67 to 31 dB. Therefore, to boost the overall harmonic rejection in the presence of such a mismatch, adding a 2nd harmonic rejection stage is beneficial. As can be seen in Fig. 6, 56 dB of harmonic rejection is achieved for the third harmonic even with 10% mismatch in both LNA and baseband gain. The results in Fig. 6 are an overestimation of HR degradation in the presence of system mismatches. In real circuit, there are other mismatches sources as well and the achieved overall HR is due to a cumulative effect of all these mismatches.

Fig. 6. Behavioural simulation results of cross-coupled baseband amplifier gain mismatch on the combined 1st and 2nd stage harmonic rejection for the 3rd LO harmonic.

III. NEAR-BAND BLOCKER SUPPRESSION

In order to improve the near-band blocker attenuation, we propose a 3rd-order baseband filtering stage as shown in Fig. 7. The response is implemented with a 3rd-order feedback impedance, where the equivalent inductance has been implemented with gyrator transconductors for on-chip fabrication. The created response works in conjunction with N-path filtering to create a sharp 3rd-order band-pass response at the LNA output. This enables an improved near-band blocker linearity while maintaining higher impedance for the in-band, resulting in smaller input referred noise from the baseband.

For such an integrator, finding precise values of circuits parameters such as C_F and C_L requires detailed analysis, resulting in a complicated 3rd-order transfer function. Such a function does not lead to any intuitive design guidelines for the integrator. Therefore, we resort to approximate design equations inferred from a pole-zero analysis of the exact transfer function. Though approximate, these equations provide simple design guidelines for the 3rd-order integrator. We later confirm that our approximate design equations reasonably match with the simulated response with small deviation.

The pole-zero analysis of the exact 3rd-order transfer function reveals that the response is mainly due to one real and two complex poles. There is also an additional zero pair in the system whose proximity with complex poles affects the response. To attain the desired response, complex poles should be placed at the required baseband bandwidth (f_{BW}). By placing a real pole at f_{BW} , the approximate required value of C_F can be calculated as:

$$C_F \approx \frac{1}{\pi f_{bw}(R_{obb} + R_{in})}, \quad (7)$$

where R_{obb} represents the baseband transconductor output resistance and R_{in} represents the equivalent of mixer and LNA output impedance, as shown in Fig. 7(b), given as:

$$R_{in} = \frac{R_{SH}(R_{oLNA} + R_{SW})}{R_{oLNA} + R_{SW} + R_{SH}}, \quad (8)$$

where R_{SH} represents the power lost due to upconversion by the harmonics of the LO. R_{SH} can be derived for our proposed 6-phase harmonic rejection mixers as $R_{SH} = 2.65(R_{SW} + R_{oLNA})$ [20].

Fig. 7. a) Single ended equivalent circuit of implemented 3rd-order integrator and b) its small-signal model.

Fig. 8. Simulated response of 3rd-order integrator for the calculated values of C_F , C_L and R_L . top) baseband response and bottom) upconverted RF response.

Similarly, by placing the complex pole pair at f_{BW} , C_L value can be calculated. However, finding the exact equation for the complex pole pair is not straightforward. Therefore, we use an indirect method by tuning the complex pole-pair frequency to f_{BW} by controlling the 3rd-order integrator complex zero-pair frequency derived as:

$$f_z = \frac{1}{2\pi\sqrt{2C_FC_L/g_{mL}^2}}. \quad (9)$$

Because this pole and zero pair frequencies lie in close proximity, changing one modifies the other one with reasonable accuracy. The integrator will only be able to maintain a 3rd-order slope in the frequency range located before its unity gain frequency. Therefore, if we place f_z around the integrators unity gain frequency, the position of the complex pole pair can be adjusted to the required f_{BW} by changing f_z . For such a case the required value of C_L can be approximated as:

$$C_L \approx \frac{g_{mL}^2}{8C_f(\pi f_{BW}(2A_{opendB}/slopedB))^2}, \quad (10)$$

where g_{mL} represents the transconductance of the gyrator transconductors, A_{opendB} represents the required voltage gain in dB from the integrator and $slopedB$ is the desired 18 dB/octave slope from 3rd-order integrator.

The calculated values of C_F and C_L will result in a transfer function with peaking. To reduce the peaking in transfer function, a series resistor R_L is added to the gyrator. Its value can be approximated as:

$$R_L \approx 1/g_{mL} + 1/(R_{oL}g_{mL}^2). \quad (11)$$

where $R_{oL} = R_{oLfb} = R_{oLff}$ represents the gyrator transconductors output impedance.

To evaluate the above design equations, we design a 3rd-order integrator for a given $f_{BW} = 10$ MHz. We use the extracted transconductances and output resistances of the proposed front-end as a starting point. $R_{oLNA} = 500 \Omega$, $R_{SW} = 10 \Omega$, $g_{mL} = 24$ mS, $R_{obb} = 2$ k Ω , $g_{mL} = 2.6$ mS, $R_{oL} = 100$ k Ω and $A_{opendB} = 33$ dB. The baseband amplifier transconductance g_{mL} was chosen to be much higher than gyrator transconductance g_{mL} to reduce its noise contribution. On the other hand, a low g_{mL} does not influence overall input referred integrator noise due to the filtering effect of C_F , and can thus be made low to reduce power consumption. Once these transconductances have been selected, output resistance values of transconductors are a consequence of amplifier structure and transistor aspect ratio in the given CMOS technology. For the rest of the parameters, value of R_{SW} should be made small as possible for adequate blocker suppression at far-away offsets. $R_{SW} = 10 \Omega$, is a compromise between blocker attenuation and LO power consumption.

With these chosen design variables, the values of C_F , C_L and R_L are calculated to be 13.5 pF, 4.75 pF and 43 Ω respectively. Fig. 8 depicts the simulated 3rd-order transfer function for the selected values. The simulated cut-off frequency of the 3rd-order integrator is about 8 MHz, compared to our initial target of 10 MHz. This deviation is expected as approximate

design equations are an over-simplified form of 3rd-order transfer function. Nevertheless, the equations provide a simple design procedure for the 3rd-order integrator and establish initial estimates for C_F , C_L and R_L values. The Final transfer function can then be tweaked in simulations to achieve exact f_{BW} .

IV. IMPLEMENTED RECEIVER

Fig. 9 presents a detailed circuit diagram of the implemented harmonic rejection receiver. The architecture uses three baseband downconversion paths, each of which is 60° degrees phase shifted from the adjacent path. In the implemented receiver, a conventional LO clocking (grey clocking arrangement in Fig. 9) was also implemented. The conventional LO clocking differs from the proposed HR LO clocking by connecting both LNA's simultaneously to a single baseband downconversion path. Thus, increasing LNA equivalent transconductance and reducing the time when overlapping can occur. With this arrangement around 3dB improvement in front-end NF is observed in measurements. Such a LO clocking can be used in the absence of 3rd harmonic blockers.

In order to measure the RF front-end performance and first stage harmonic rejection, a test signal from the output of the first baseband amplifier was routed outside the IC. RF performance was then measured by buffering this signal with an external operational amplifier and observing the response at the output measurement point. The second stage harmonic rejection was followed by a second order delta-sigma ADC with a 3bit quantizer and current-steering DAC's in the feedback path. The output of the delta-sigma ADC was seven bit thermal, which in turn was converted to three bit binary and then routed outside the IC through LVDS buffering. In the following, we will explain the design details of various sub-block of the proposed receiver.

A. LNA and Downconversion Mixing

Fig. 10(a) shows the circuit diagram of the implemented LNA [21]. The LNA consists of common-gate and common-source amplifiers, where the common source amplifier is added to increase the gain and output impedance of the LNA as compared to resistive loads. Higher output impedance is required for a proper functioning of the N-path filtering as it affects the relative blocker attenuation [22]. Resistors R_1 and R_2 provide the necessary dc-biasing while resistors R_3 - R_6 are added to sense the dc-bias voltage for the common mode feedback loop. The designed common-mode feedback loop ensures that the output common-mode voltage at *outp/outn* is set at $V_{dd}/2$, which creates an optimum output swing range. Capacitors C_a and C_b create capacitive feedback that acts in conjunction with upconverted 3rd-order filtering response at the LNA output nodes to create a similar 3rd-order input impedance profile at the LNA input. The benefit is that the input impedance is tunable through f_{LO} and can be easily matched to the input source impedance by adjusting the capacitive feedback ratio set by C_a and C_b .

A simplified form of the input impedance (Z_{in}) can be derived by neglecting the parasitic capacitances and common-gate common-source output impedances. The derived equation

helps in crudely establishing circuit behavior in terms of the main design parameters:

$$Z_{in} \approx \frac{1}{gm_{cg}(1 - \beta gm_{cs} Z_L(\omega))} + \frac{\beta Z_L(\omega)}{1 - \beta gm_{cs} Z_L(\omega)}, \quad (12)$$

where gm_{cg} represents the small signal transconductance of the common-gate amplifier, gm_{cs} represents the transconductance of the common-source amplifier, $Z_L(\omega)$ represents the 3rd-order upconverted load impedance seen by the LNA,

$$Z_L(\omega) \approx (R_{oLNA} + R_{SW}) || R_{SH} || Z_{3rd}, \quad (13)$$

while β represents a capacitive feedback ratio given by:

$$\beta \approx \frac{C_a + C_{gd,cg}}{C_a + C_{gd,cg} + C_b}. \quad (14)$$

where R_{oLNA} represents the output resistance of the LNA, Z_{3rd} is the input impedance of the 3rd-order integrator and $C_{gd,cg}$ represents the combined parasitic gate-to-drain capacitance of M_{CG} .

The derived Z_{in} suggests that if the LNA is loaded with a bandpass filtering response at RF, i.e., high impedance at the desired frequency and low impedance at blocker frequencies, then the impedance at the blocker frequencies will be roughly equal to $1/g_{cg}$, while at the desired frequency the input impedance can be matched to the source impedance by tuning β , $Z_L(\omega)$, and gm_{cs} . Ideally, providing a low impedance at the third harmonic blockers will also help in blocker suppression. However, due to device parasitics, providing a low impedance across a wideband range covering the third harmonics is a design challenge and was not done in the proposed design. In a similar manner, voltage gain (A_{vRF}) of LNA can be derived as:

$$A_{vRF} \approx \frac{2(gm_{cg} + gm_{cs})Z_L(\omega)}{1 + gm_{cg}[\beta Z_L(\omega) + R_S - gm_{cs}\beta R_S Z_L(\omega)]} \quad (15)$$

Equation. 16 suggests that if we keep gm_{cg} and gm_{cs} constant, LNA gain can be controlled mainly through $Z_L(\omega)$ and β . The LNA's are loaded with 6-phase down-conversion passive mixers and a 3rd-order baseband stage. The transparent nature of passive mixers up-converts the low-pass input impedance of the 3rd-order integrator stage to a band-pass impedance at mixer RF nodes. This impedance, in turn, acts as a load for LNA, creating a 3rd-order RF band-pass filter tunable through the f_{LO} .

B. Phase/Frequency and Offset Tuning

The parasitic capacitance present at the LNA output makes the LNA output impedance complex in nature. That creates a phase/frequency offset in the N-path filtering response, making it's center frequency drift away from f_{LO} [23]. To tune the N-path center frequency back to f_{LO} , we implement a transconductor-based feed-forward path across three baseband paths: $\sin 0^\circ/60^\circ/300^\circ$. Modified from the concept described in [24], the implemented phase/frequency tuning arrangement is illustrated in Fig. 11 where the feed-forward transconductors

Fig. 9. Detailed block diagram of the implemented harmonic rejection receiver.

re-adjust the phase/frequency profile. To visually understand the functionality of phase/frequency tuning, a phasor diagram of the three baseband paths is drawn in Fig. 11. The original vector shown by the dotted lines undergoes a phase/frequency shift creating vectors represented by the solid lines. Phase and frequency are then readjusted by adding/subtracting adjacent baseband path signals with a multiplication factor α , controlled through the transconductance of the feed-forward transconductors.

Another parameter that needs adjustment is the dc-offsets at the input of the first baseband amplifiers. Generated by device mismatches and circuit unsymmetries, offset can be quite devastating in direct downconversion receivers. As shown in

Fig. 11, to adjust the dc-offset we implement differential current sources O_1 , O_2 and O_3 , which source current from one node and sink from another thus reducing the dc-offset from the differential inputs of the first baseband amplifier.

C. Baseband Amplifiers

Fig. 10(c) shows the circuit diagram of the implemented dynamically-biased baseband transconductors. Transistors M_1 - M_4 constitute a simple differential pair which is biased through M_5 - M_{10} . Transistors M_5 and M_6 dynamically increase the bias current of the main differential amplifier for a larger input signal. The outputs of the differential amplifier are

Fig. 10. Implemented circuits: a) LNA, b) baseband amplifier, c) passive mixer, and d) proposed multi-output LO generator parameterized for K outputs.

Fig. 11. Phasors illustrating the correction of phase/frequency offset at LNA output due to complex load impedance.

kept at the desired common-mode voltage through a common-mode feedback created by M_{11} - M_{15} .

All baseband amplifiers are designed with the same configu-

ration, with the small exception of designing the first baseband transconductor with a bias current of 3.8 mA. This is about ten times higher the bias currents of later baseband stages to ensure a reduced noise contribution from the first baseband amplifier.

D. 3rd-order Integrator

Fig. 7 and 9 show the implemented 3rd-order integrator. The main baseband amplifier is implemented with a higher transconductance of 23 mS, as compared to gyrator transconductance of 2.6 mS. This is to ensure reduced input referred noise of the main baseband amplifier. The simulated input referred noise the the gyrator averaged over 10 MHz baseband bandwidth was 8.8 nV. Nevertheless, the filtering capacitors C_F attenuated the noise from the gyrator at low frequencies and therefore, the effect of gyrator noise on overall noise performance was only a small percentage. The values of capacitors C_f and C_L are tunable through a switched capacitor matrix to adjust the integrator response at the desired bandwidth. The implemented integrator together with N-path

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work	[14]	[13]	[18]	[26]	[15]
Frequency (GHz)	0.7-2	0.2-1	0.1-2.4	0.7-1.4	0.1-3	0.4-6
HR @ 1st gain stage (dB)	18-37	20	NA	NA	NA	NA
Overall HR (dB)	46-53	51-52	52-54	40-67	45 ⁽¹⁾	>40 ⁽¹⁾ / ⁽²⁾ >75 ⁽³⁾
Architecture	LNA first	LNA first	Mixer first	LNA first	Mixer first	LNA first
N-path phases	6-phase	8-phase	8-phase	8-phase	32-phase	8-phase ⁽³⁾ /4-phase ⁽⁴⁾
f_{BW} (MHz)	10	2	0.2-3	10	NR	0.5-50
BCP (dBm)	-1 to -5@ $10f_{BW}$	-2.4@ $10f_{BW}$	-6 to 2.5@ $27f_{BW}$	-8.5 to 10@ $10f_{BW}$	$\approx$ -11	NR
BCP@ $3f_{LO}$ (dBm)	2.5@ $10f_{BW}$	-2.8	-8	NR	$\approx$ -15	NR
Near band BCP (dBm)	-6.5@ $4f_{BW}$	NR	NR	NR	NR	NR
Noise Figure (dB)	5-11	5.4-6	1.7	1.5-8	2.4-5	1.8 to 3.1
BNF (dB)	13-17 ⁽⁵⁾	NR	9@-5dBm ($3f_{LO}$)	6.6-7.9@-9dBm	9-11@-5dBm	10-14
OB IIP3 (dBm)	8-11@ $10f_{BW}$	9@ $10f_{BW}$	10	1-20.5@ $10f_{BW}$	4	>8/>3 ⁽⁶⁾
Gain (dB)	36	36	NR	20.8-36.8	42	58-70
Power (mW) @ Vdd (V)	54@1	26-32@1.2, 2.5	36.8-62.4@1	52@ 0.8, 1, 1.2	28-31@NR	< 40@0.9
Process	28nm FDSOI	65 nm	28 nm	65 nm	28nm	28 nm

NR: not reported, NA: not applicable. 1) without calibration 2) with calibration 3) for 0.4-3 GHz 4) for 3-6 GHz 5) simulated 6) different configurations

filtering creates a 3rd-order bandpass filtering response at the LNA output thereby suppressing near-band blockers.

E. LO and Sampling Frequency Generation

Fig. 10(d) shows the proposed multi-output LO generator utilized in this work to create sampling waveforms. The primary motivation for the proposed concept is on-chip scalability with respect to the number of driven mixers. For instance, in Fig. 10(d) the schematics are parameterized for $2K$ outputs, meaning that 2-, 4- ... $2K$ -phases mixers can be driven from this generator according to the divider control word (dcw).

The proposed multi-output generator can be partitioned into the three main functional blocks: waveform synthesizer, associated propagation network, and a pulse slicer. First, the waveform synthesizer divides incoming clock to create a lower frequency 50% duty-cycle waveform. The synthesized waveform is then fed to propagation network for re-clocking via dummy flip-flop (DMY) and is further cycle-by-cycle shifted to maintain timing between the network taps. Finally, pulse slicer utilizes propagation network taps to construct non-overlapping $1/2K\%$ duty-cycle pulse streams via logic gates. Better than multi-output generation based on analog delay cells in [25], pulse slicing with D-flip-flop scales with the clock frequency and does not require an analog tuning loop.

In the implemented prototype with $K = 3$ to generate 6-phase LO, an external signal with the frequency of $3 \times f_{LO}$, was routed to LO-generation first stage (Enabler in Fig. 10(d)) through resistive feedback buffers. Resistive feedback ensures input matching for the external clock signal, while the enabler block brings the signal to the digitally compatible levels. The latter allows the all-digital implementation of LO-generator, meaning HDL-described functionality and automatic place-and-route.

V. MEASUREMENT RESULTS

The proposed receiver was fabricated in a 28nm FDSOI technology for an operating frequency of 0.7-2 GHz. In order to utilize the bodybias features of the FDSOI technology, the bodybias of NMOS transistors was tied to supply voltage to

Fig. 12. Chip photograph of the proposed harmonic rejection receiver.

reduce their threshold voltage. The chip photograph of the complete receiver IC is presented in Fig. 12. The chip area is 2.16mm^2 .

Fig. 13 shows the measured noise figure (NF) and harmonic rejection from the first and second harmonic rejection stage outputs. Without any calibration, harmonic rejection in the range of 18 to 37 dB is observed from the first stage, while combined harmonic rejection from the first and second stage ranges from 46-53 dB as measured from ADC output. The measured noise performance is limited in the high-end of the frequency range by non-optimal overlapping of the LO waveforms in the measured prototype.

A conventional LO clocking was also implemented in the proposed design where each baseband branch is only connected to one LNA at a time (grey clocking arrangement in Fig. 9), thus increasing LNA equivalent transconductance and reducing the time when overlapping can occur. With this arrangement around 3 dB improvement in front-end NF is observed in measurements. Such a LO clocking can be used in the absence of 3rd harmonic blockers.

Fig. 14 plots the 3rd-order baseband filtering response, out-of-band (OB) IIP3 and blocker 1 dB gain compression points (OB P1dB) versus baseband frequency offset. Out-of-band IIP3 and P1dB are measured for both the front-end and complete receiver where the receiver front-end linearity

Fig. 13. NF and the harmonic rejection from the first and second stage of the proposed receiver, for harmonic rejection LO clocking (black) and conventional LO clocking (grey).

Fig. 14. Baseband filtering response, IIP3 and P1dB compression point of front-end (FE) and receiver (RX) for an $f_{LO} = 1.5$ GHz.

measures are higher than the receiver. One can observe 3rd-order filtering near the baseband bandwidth (f_{BW}) of 10 MHz. This 3rd-order response is upconverted to the LNA output nodes with N-path filtering and helps to suppress near-band blockers. For example, the measured P1dB compression point from front-end output for a near-band blocker located at a 40 MHz offset from f_{LO} is -6.5 dBm which is just 1.5 dB less than P1dB measured at a 100 MHz offset. In the measured baseband filtering response, the attenuation for blockers above 40 MHz is lower than behavioural simulation results in Fig. 8. This was mainly due to higher observed mixer switch resistance in the measurements. Moreover, at higher offsets the unity gain bandwidth of the 3rd-order baseband filter is reached and after that frequency, it is not possible to provide a 3rd-order filtering response. To observe the receiver linearity behavior across the operating frequency, Fig. 15 shows the measured OB IIP3 and P1dB versus frequency for a blocker at a 100 MHz offset from f_{LO} .

For observing linearity in the presence of blockers at $3f_{LO}$, P1dB was measured with three offset frequencies, 100 MHz, 40 MHz and 4 MHz. These three offsets represent downconversion of the blocker to out-of-band, near-band, and in-band reception frequencies. The measurement was performed by sweeping the blocker power and determining the P1dB point of the receiver. As shown in Fig. 16, we observe P1dB points of -7, 1 and 2.5 dBm respectively, achieving state-of-the-art results [13], [14]. The measurement was done from the front-end test output to clearly demonstrate blocker suppression from the

Fig. 15. OB IIP3 and P1dB versus receiver operating frequency. The blocker is placed at $f_{LO}+100$ MHz.

Fig. 16. Measured signal gain under the presence of a strong blocker at $3f_{LO}$. For a blocker at $3f_{LO}+100$ MHz, blocker P1dB of 2.5 dBm is observed.

Fig. 17. Measured input matching at $f_{LO} = 0.7, 1, 1.5$ and 2 GHz.

first harmonic rejection stage.

Fig. 17 shows the measured S_{11} across various input frequencies inside the receiver band of 0.7-2 GHz. As expected, a good input match is achieved and can be tuned to the desired frequency through change of f_{LO} .

VI. CONCLUSION

Blocker tolerance is one of the key specifications for modern wideband receivers. In this paper, we have proposed a blocker tolerant harmonic rejection receiver which is able to efficiently suppress blockers at local oscillator harmonics together with suppression of near-band blockers. This is achieved by implementing harmonic rejection in two stages, so that harmonic rejection begins already at the output of the first gain stage. In addition, a 3rd-order baseband impedance is

$$\frac{V_o}{V_i} = \frac{R_{obb}(L_L C_F^2 s^3 + (R_L C_F^2 - 2L_L g_{mbb} C_F) s^2 - 2R_L g_{mbb} C_F s - g_{mbb})}{1 + (2C_F R_L + C_F R_{in} + C_F R_{obb}) s + \alpha s^2 + \beta s^3}, \quad (16)$$

$$\alpha = 2C_F L_L + C_F^2 R_L R_{in} + C_F^2 R_L R_{obb} + C_F^2 R_{in} R_{obb} + C_F^2 R_L R_{in} R_{obb} g_{mbb}, \quad (17)$$

$$\beta = C_F^2 L_L R_{in} + C_F^2 L_L R_{obb} + C_F^2 L_L R_{in} R_{obb} g_{mbb}. \quad (18)$$

implemented, which acts in conjunction with N-path filtering for near-band blocker attenuation. The proposed architecture uses only six local oscillator phases and baseband paths and achieves harmonic rejection with simple gain coefficients of ± 1 . Measured results from a fabricated prototype in 28 nm FDSOI technology demonstrate 18-37 dB harmonic rejection from the first stage and 46-53 dB of harmonic rejection from the first and second stages. The near-band blocker compression point of is -6.5 dBm and an BCP of 2.5 dBm for third harmonic blocker measured from RF test output.

APPENDIX A

THIRD-ORDER INTEGRATOR STABILITY ANALYSIS

Based on the small signal model of third-order integrator presented in Fig. 7, the integrator transfer function can be derived and is provided in Eq. 16. In the derived transfer function, R_{in} is given by Eq. 8 and $L_L = C_L / g_{mL}^2$.

The derived transfer function can be utilized to observe the stability limits of the design. To do so we evaluate the derived transfer function for the practical circuit parameters provided in Section III. Different circuits parameters are swept while keeping others to their default values. Fig. 18 to 21 plot the root-locus of the transfer function when R_L , R_{oLNA} , C_F and, C_L values are swept. The plots indicate that for the chosen circuit parameters from Section III, $R_{oLNA} > 8 \text{ k}\Omega$, $C_F < 7 \text{ pF}$ and $C_L > 17 \text{ pF}$ will bring the dominant poles to the right side of pole-zero plot making the system unstable.

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Fig. 18. Root-locus plot of third-order transfer function when R_L is swept from $0 \text{ }\Omega$ to $10 \text{ k}\Omega$. R_L values close to $0 \text{ }\Omega$ and $10 \text{ k}\Omega$ bring the integrator at the verge of instability.

Fig. 19. Root-locus plot of third-order transfer function when R_{oLNA} is swept from $50 \text{ }\Omega$ to $8 \text{ k}\Omega$.

Fig. 20. Root-locus plot of third-order transfer function when C_F is swept from 5 pF to 50 pF.

Fig. 21. Root-locus plot of third-order transfer function when C_L is swept from 2 pF to 17 pF.

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Faizan Ul Haq (S'12) received his M.Sc. and PhD degrees in electrical engineering from Tampere university Finland and Aalto University Finland in 2012 and 2019. From 2012-2014 he was working as a research intern in Nokia research center, Finland. He is currently working as a senior design engineer at CoreHW Finland. His research interests include RF/analog communication circuits and power management circuits such as dc-dc converters.

Mikko Englund was born in Espoo, Finland, in 1985. He received the M.Sc. and PhD degrees in electrical engineering from Aalto University School of Electrical Engineering, Espoo, Finland in 2013 and 2018. He is currently working as a senior RFIC design engineer at Huawei technologies Finland. His research interests include filters and high-speed analog-to-digital converters in digital-intensive receivers.

Marko Kosunen received his M.Sc., L.Sc. and D.Sc. (with honors) degrees from Helsinki University of Technology, Espoo, Finland, in 1998, 2001 and 2006, respectively. He is currently a Senior Researcher at Aalto University, Department of Electronics and Nanoengineering. Academic years 2017-2019 he visited Berkeley Wireless Research Center, UC Berkeley, on Marie Skłodowska-Curie grant from European Union. He has authored and co-authored more than 80 journal and conference papers and holds several patents. His current research interests include programmatic circuit design methodologies, digital intensive and time-based transceiver circuits, and medical sensor electronics."

Yury Antonov (S'15) received the Engineering degree in computer design and technology from Bauman Moscow State Technical University (BMSTU), Moscow, Russia, in 2007, and the M.Sc. degree (Hons.) in electrical engineering from Aalto University, Espoo, Finland, in 2014, where he is currently pursuing the Ph.D. degree. From 2004 to 2010, he was a Circuit Designer with several research and development companies in Moscow, where he was developing CPLD/FPGA-based mixed-signal circuits for the synchronization of scalable radar-phased arrays and designing downconversion front ends for lidar-based measurement solutions. He is now with Aalto University, where he has worked on multiple successful tape-outs from 28 to 65 nm. His research interests are in multi-phase and spur-free frequency synthesis for RF/mm-wave front ends with digital assistance and on-chip calibration loops. Mr. Antonov has served as a reviewer and co-reviewer for a number of international journals and conferences. He was a recipient of the Best Student Paper Award from the 22nd European Conference on Circuit Theory and Design.

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Kim B. Östman received the M.Sc. (with distinction) and Lic. Tech. degrees from Tampere University of Technology, Tampere, Finland, in 2005 and 2012, respectively, and the D.Sc. (with honors) degree from Aalto University, Espoo, Finland, in 2014. He also holds the Ph.D. degree in the humanities from Åbo Akademi University, Turku, Finland. He was with the Department of Communications Engineering at Tampere University of Technology from 2002 to 2010, and with the Department of Micro- and Nanosciences at Aalto University School of Electrical Engineering from 2011 to 2014. From 2014 to 2015, he was with Nokia Technologies, and is now with Nordic Semiconductor as a Senior R&D Engineer. His research interests include highly linear wireless CMOS receivers, with a particular emphasis on digital-intensive solutions, along with frequency synthesizers and fully integrated DC-DC conversion.

Miikka Tenhunen was born in Helsinki, Finland, in 1995. He received his B.Sc. degree in electrical engineering from Aalto University School of Electrical Engineering, Espoo, Finland, in 2018. He is currently a master's student with Micro- and Nanoelectronic Circuit Design as his major. He is working as an assisting researcher at the Department of Electronics and Nanoengineering, Aalto University School of Electrical Engineering.

Kimmo Koli (M'95) was born in Karuna, Finland, in 1964. He received the M.Sc., Lic. Tech., and D.Sc. degrees in electrical engineering from the Helsinki University of Technology, Helsinki, Finland, in 1991, 1995, and 2000, respectively. From 1989 to 2000, he was a Research Engineer in Electronic Circuit Design Laboratory at the Helsinki University of Technology. From 2000 to 2008, he was a Principal Scientist at Nokia Research Center, Helsinki, Finland, working on audio and sensor interfaces and wireless transceivers. From 2008 to 2014, he joined STMicroelectronics (later ST-NXP Wireless, ST-Ericsson, and Ericsson) and is currently with HiSilicon at Huawei Technologies Oy (Finland) Co. Ltd., Helsinki, Finland, focusing on RF design blocks for wireless applications. He has authored or coauthored over 40 journal articles and conference papers and holds over 10 patents. Dr. Koli served as a member of the technical program committee of IEEE International Solid-State Circuits Conference from 2011 to 2014 and IEEE European Solid-State Circuits Conference since 2011.

Kari Stadius (S'95-M'03) received the M.Sc., Lic. Tech., and Doctor of Science degrees in electrical engineering from the Helsinki University of Technology, Helsinki, Finland, in 1994, 1997, and 2010, respectively. He is currently working as a staff scientist at the Department of Electronics and Nanoengineering, Aalto University School of Electrical Engineering. His research interests include the design and analysis of RF transceiver blocks with special emphasis on frequency synthesis, and for analog and mixed-mode circuit design. He has

authored or coauthored over 70 refereed journal and conference papers in the areas of analog and RF circuit design.

Jussi Ryyänen (S'99-M'04-SM'16) was born in Ilmajoki, Finland, in 1973. He received his Master of Science, Licentiate of Science, and Doctor of Science degrees in electrical engineering from Helsinki University of Technology (HUT), Helsinki, Finland, in 1998, 2001, and 2004, respectively. He is currently working as an associate professor at the Department of Electronics and Nanoengineering, Aalto University School of Electrical Engineering. His main research interests are integrated transceiver circuits for wireless applications. He has authored or coauthored over 100 refereed journal and conference papers in the areas of analog and RF circuit design. He holds six patents on RF circuits