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ABSTRACT
Thermally varying hysteretic gate operation in few-layer ReS$_2$ and MoS$_2$ back gate field effect transistors (FETs) is studied and compared for memory applications. Clockwise hysteresis at room temperature and anti-clockwise hysteresis at higher temperature (373 K for ReS$_2$ and 400 K for MoS$_2$) are accompanied by step-like jumps in transfer curves for both forward and reverse voltage sweeps. Hence, a step-like conductance (STC) crossover hysteresis between the transfer curves for the two sweeps is observed at high temperature. Furthermore, memory parameters such as the RESET-to-WRITE window and READ window are defined and compared for clockwise hysteresis at low temperature and STC-type hysteresis at high temperature, showing better memory performance for ReS$_2$ FETs as compared to MoS$_2$ FETs. Smaller operating temperature and voltage along with larger READ and RESET-to-WRITE windows make ReS$_2$ FETs a better choice for thermally aided memory applications. Finally, temperature dependent Kelvin probe force microscopy measurements show decreasing (constant) surface potential with increasing temperature for ReS$_2$ (MoS$_2$). This indicates less effective intrinsic trapping at high temperature in ReS$_2$, leading to earlier occurrence of STC-type hysteresis in ReS$_2$ FETs as compared to MoS$_2$ FETs with increasing temperature.

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Recently, two-dimensional (2D) layered materials have attracted significant research interest for memory applications. Thermally assisted non-volatile memories (NVMs) have been demonstrated using monolayer and few-layer MoS$_2$.

In several other reports, large hysteresis in transistor transfer curves, normally undesirable for device performance, has been utilized for NVM applications. All of these reports use MoS$_2$ as the channel or as the charge trapping layer. In thermally assisted NVMs, locally generated heat is exploited for switching between different memory states. MoS$_2$ has shown excellent switching characteristics compared to other transition metal dichalcogenides (TMDs). Low off current ($I_{off}$) and a high on/off current ($I_{on}/I_{off}$) ratio (due to a large bandgap) along with a low sub-threshold slope and high effective mass are some of the advantages of MoS$_2$, which make it a desirable switching material for memory applications.

Among the TMDs, ReS$_2$ has also garnered significant attention recently since it behaves as decoupled monolayers stacked on top of each other due to the lack of interlayer coupling and weak interlayer registry. Hence, ReS$_2$ remains a direct bandgap semiconductor ($E_g = 1.5$ eV) from monolayer to bulk, showing no direct to indirect bandgap crossover as is shown by other TMDs, making it a preferred material for optoelectronic applications.

With the increasing packing density of field effect transistors (FETs) on a single wafer, high performance ICs can reach an operating temperature ($T$) of 370–530 K (Ref. 14), making it important to understand and exploit the changes that occur in the properties of 2D materials at high $T$. Thermally assisted memory is one such application where locally generated heat is exploited to aid the switching between RESET (RST/STATE 0) and WRITE (WR/STATE 1) states. It can enable embedded in-memory computing that has emerged as a key hardware bottleneck for artificial intelligence/machine learning technologies. However, in-memory computing requires more computational power per unit volume of data storage in the RAM and parallel
TABLE I. Comparison of memory parameters obtained in this work with the previous reports on thermally assisted memory using MoS2 as the channel material.

<table>
<thead>
<tr>
<th>References</th>
<th>Material</th>
<th>Operating temperature (°C)</th>
<th>Operating voltage (V)</th>
<th>RST-to-WR window (ΔVth/Vpp)</th>
<th>RD window (ΔVth/Vpp)</th>
<th>Hysteresis type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Monolayer, MoS2</td>
<td>490</td>
<td>-40 V to +40 V</td>
<td>0.44</td>
<td>5.5</td>
<td>STC + ACW</td>
</tr>
<tr>
<td>21</td>
<td>Monolayer, MoS2</td>
<td>350</td>
<td>-30 V to +15 V</td>
<td>0.50</td>
<td>7</td>
<td>CW</td>
</tr>
<tr>
<td>22</td>
<td>Multilayer MoS2</td>
<td>300</td>
<td>-30 V to +30 V</td>
<td>0.1</td>
<td>—</td>
<td>CW</td>
</tr>
<tr>
<td>This work</td>
<td>Few-layer MoS2</td>
<td>400</td>
<td>-100 V to +60 V</td>
<td>0.16</td>
<td>1.9</td>
<td>STC + ACW</td>
</tr>
<tr>
<td>This Work</td>
<td>Few-layer ReS2</td>
<td>375</td>
<td>-100 V to +30 V</td>
<td>0.58</td>
<td>7.4</td>
<td>STC + ACW</td>
</tr>
</tbody>
</table>

All the measurements reported in this work start with the FS followed by RS. We observe two significant step-like jumps in the G-Vth plots at higher T. The first one occurs during FS at 20 V for ReS2 [Fig. 1(d)] and at 35 V [Fig. 2(d)] for MoS2. The second one occurs during RS at -76 V for ReS2 [Fig. 1(d)] and -66 V for MoS2 [Fig. 2(d)]. As a result STC hysteresis emerges at 373 K and 400 K for ReS2 and MoS2, respectively. These jumps can be prominently observed in the trans-conductance (g_m) curves in Figs. 1(a) and 1(b) of the supplementary material for ReS2 and MoS2, respectively. Along with the jumps occurring at higher T, a switch from CW hysteresis at RT to ACW hysteresis at higher T can also be observed in the transfer curves for both ReS2 and MoS2.

The changing hysteresis behavior with varying T is shown in Figs. 3(a) and 3(b) via the change in threshold voltage (Vth) for FS (STATE 1, Vth^FS) and RS (STATE 0, Vth^RS) with T for MoS2 and ReS2, respectively. A transition from CW (Vth^FS < Vth^RS) to ACW (Vth^FS > Vth^RS) hysteresis with increasing T can be observed. A larger hysteresis width (ΔVth = Vth^FS - Vth^RS) for ReS2 at much lower T compared to MoS2 can also be seen. As marked in Figs. 1(d) and 2(d), WR and RST operations are carried out at the end of FS and RS, respectively. A larger ΔVth implies a larger RST-to-WR window, a desirable feature for distributed processing. This increases the operational T of data centers, resulting in several reliability concerns. Therefore, enabling low T memory operation in 2D materials is timely and relevant. In this study, thermally varying hysteretic gate operation, in few-layer MoS2 and in few-layer ReS2, is studied and compared for memory applications. Four-terminal back gate FETs are used in this study to eliminate the contribution from contact resistance. Clockwise (CW) hysteresis is observed for both ReS2 and MoS2 at room temperature (RT), whereas anti-clockwise (ACW) hysteresis along with step-like jumps in the transfer curves leading to a conductance crossover during the forward sweep (FS, -100 V to +100 V) and reverse sweep (RS, +100 V to -100 V) directions (step-like conductance crossover hysteresis or STC hysteresis) is observed at high T. A similar behavior has been previously reported for monolayer MoS2 FETs. Here, we observe this behavior in both few-layer MoS2 at 400 K and few-layer ReS2 at 375 K, attributing the RT CW hysteresis to the dominance of native intrinsic traps and the conductance crossover at high T to charge exchange between the p’ Si back gate and gate oxide SiO2. The charge can be trapped in the oxide near the 2D channel/dielectric or the back gate/dielectric interface. However, the latter is found to be dominating at high T in these systems. A comparison of this work with previous reports on thermally assisted memory is presented in Table I.

We observe lower operating voltage (Vpp), a larger RST-to-WR window, defined as ΔVth/Vpp (where ΔVth is the hysteresis width), and a larger READ (RD) window for STC hysteresis in ReS2 devices. Improved memory parameters for ReS2 FETs at much lower T are observed. Source/drain electrodes were then patterned using electron beam lithography followed by metal deposition. 10 nm Cr and 100 nm Au were used to form source/drain metal contacts with the flakes.

Figures 1 and 2 show the conductance (G) vs back gate voltage (VGS) curves for varying T. Figures 1(d) and 2(d) define the RST, RD, and WR operations for the ReS2 and MoS2 memories, respectively.
memory operation. Hence, a larger RST-to-WR window is observed for ReS$_2$ as compared to MoS$_2$. Figure 3(c) shows the ratio of $g_m$ closer to STATE 0 and STATE 1.25. The change in $V_{GS}$ during memory operation during FS is shown in Fig. 4(c), depicting the inversion from CW to ACW hysteresis with increasing $T$ for ReS$_2$ at all voltages due to the availability of thermionic energy. When $T$ is increased from RT to higher $T$, a change from CW to ACW hysteresis is seen at RT. At higher $T$, the deep level traps have an equal probability of getting trapped irrespective of the voltage applied, and hence, the hysteresis starts to fade away. Instead, an ACW hysteresis with step-like jumps in the $G$ vs $V_{GS}$ profile starts occurring at $348$ K for ReS$_2$ and at $373$ K for MoS$_2$, which is attributed to the trapping and de-trapping of $e^-$ from the gate into the oxide and vice versa with enough activation energy ($E_a$) at higher temperature. At high $T$, at the beginning of FS ($V_{GS} < 0$), the bands bend as shown by the schematic in Fig. 3(d)–(iii) favoring $e^-$ injection from the gate into the oxide causing gate field screening. The stored $e^-$ give rise to a repulsive field in addition to the gate field as long as $V_{GS} < 0$. For $V_{GS} > 0$, the bands evolve allowing the trapped oxide $e^-$ to jump back into the gate, resulting in a sudden increase in the attractive field seen by the channel and the first $g_m$ jump is observed, which leads to STATE 1 of the memory operation during FS. For $V_{GS} < 0$ during RS, the ejection of $e^-$ from the oxide into the gate is again favored allowing the second $g_m$ jump, leading to STATE 0 of the memory operation. It is important to note that at lower $T$, the gate $e^-$ do not have the $E_a$ required to overcome the barrier between the gate and the oxide. Hence, intrinsic trapping is the dominating mechanism responsible for CW hysteresis at lower $T$.

Figure 4(a) plots $\Delta V_{th}$ (left axis) and trap density ($\Delta N_T$, right axis) vs $T$, extracted from Figs. 1 and 2 for ReS$_2$ (red line) and MoS$_2$ (green line), respectively, using the following equation:

$$\Delta N_T = \frac{\Delta V_{th} \times C_{ox}}{q},$$

where the gate oxide capacitance per unit area is given by $C_{ox} = \frac{e_d}{d}$, $e_d$ = 3.9, and oxide thickness $d = 280$ nm. The fits (dashed lines) to $\Delta V_{th}$ and $\Delta N_T$ in Fig. 4(a) are used to extract the oxide trap density ($\Delta N_{OT}$) and intrinsic trap density ($\Delta N_{IT}$) components for ReS$_2$ and MoS$_2$ in Fig. 4(b). $\Delta N_{OT}$ is considered to be negligible at RT and the same for both ReS$_2$ and MoS$_2$ at all $T$ since both types of devices are fabricated on identical p$^+$ Si/SiO$_2$ substrates. The algebraic sum of $\Delta N_{OT}$ and $\Delta N_{IT}$ results in total $\Delta N_T$. For both materials, hysteresis becomes zero at higher $T$ due to the reducing impact of $\Delta N_{IT}$, but the effect of $\Delta N_{IT,ReS_2}$ dies faster than $\Delta N_{IT,MoS_2}$. This is explained by a schematic shown in Fig. 4(c), depicting the inversion from CW to ACW hysteresis with increasing $T$ due to the dominance of $\Delta N_{IT}$ and $\Delta N_{OT}$ independently at RT and high $T$, respectively. The evolution of hysteresis with $T$ due to only $\Delta N_{OT}$ is shown by the solid pink line, depicting a negligible hysteresis at lower $T$, which eventually increases for higher $T$. However, the solid red and blue lines show the effect of $\Delta N_{IT}$ on hysteresis for ReS$_2$ and MoS$_2$ with $T$, respectively. Hence, adding the hysteresis effects from the two kinds of traps gives the net hysteresis change as shown by the dashed lines in Fig. 4(b). Steeper reduction in $\Delta N_{IT,ReS_2}$ with $T$ as compared to $\Delta N_{IT,MoS_2}$ can be observed.
Finally, T-dependent KPFM measurements were performed to confirm the proposed model. The average contact potential difference (CPD) measured for ReS₂ and MoS₂ is shown in Fig. 4(d). We define CPD by

\[ \phi_{\text{sample}} = \phi_{\text{tip}} - [q \times \text{CPD}], \]

where \( \phi_{\text{sample}} \) and \( \phi_{\text{tip}} \) represent the work function of the sample and the tip, respectively, and \( q \) is the electronic charge. The CPD values obtained are consistent with previous reports.²⁹,³⁰ CPD values for ReS₂ increase with increasing T, whereas they remain almost unchanged for MoS₂. The temperatures for crossover from CW to ACW hysteresis are marked as \( T_{\text{CPD,ReS}_2} \) and \( T_{\text{CPD,MoS}_2} \). The material with a more negative CPD value implies a larger work function and more e⁻ trapping. As shown in Eq. (2), previous reports, gas adsorbates that act as e⁺ acceptors are responsible for e⁻ depletion, leading to more negative CPD.²⁹,³⁰ However, all the measurements in this work are carried out in a controlled nitrogen ambient, ruling out the presence of adsorbates as a possible cause for e⁻ depletion. Therefore, we infer intrinsic trapping as the likely reason for e⁻ depletion, resulting in more negative CPD values at RT for ReS₂. Moreover, intrinsic trapping can only be observed in devices with fully depleted channels;²⁹,³⁰ hence, at higher T, the effect of intrinsic traps is nullified and oxide trapping dominates. As shown in Fig. 4(d), \( T_{\text{CPD,ReS}_2} \) is less than \( T_{\text{CPD,MoS}_2} \), implying that the effect of intrinsic traps persists for much higher T in MoS₂ than for ReS₂ consistent with the proposed model. The CPD maps for ReS₂ are shown in Fig. 5(a) at 323 K and Fig. 5(b) at 373 K and for MoS₂ in Fig. 5(c) at 323 K and Fig. 5(d) at 373 K. The contrast for all the images is adjusted on the same scale, clearly showing the most negative CPD for ReS₂ at RT in Fig. 5(a).

To conclude, in this report, we demonstrate thermally assisted memory using back-gated vdP FETs with few-layer ReS₂ and MoS₂ as the channel materials. The transfer characteristics show a change in the hysteresis direction from CW to ACW with increasing T, along with step-like jumps in the transfer curves at higher T (STC crossover hysteresis). Memory parameters such as RST-to-WR and RD windows are compared for memory operation. The step-like jumps in the transfer curve occur at much lower T for ReS₂ (373 K) as compared to MoS₂ (400 K), making it a better choice for memory applications. These results are ascribed to a combined effect of intrinsic traps at lower T and screening of gate voltage due to electron injection from the gate into oxide trapping sites at higher T. This physical model is corroborated through T-dependent KPFM measurements that show an increase in CPD for ReS₂, while an almost constant CPD for MoS₂ with increasing T. This implies enhanced depletion of electrons in ReS₂ with increasing T, reinforcing the model of faster de-trapping of intrinsic ReS₂ traps with T and hence a lower crossover T.

See the supplementary material for the transconductance (\( g_m \)) vs gate voltage (\( V_{GS} \)) plots at varying temperatures for ReS₂ and MoS₂ showing jumps during forward sweep and reverse sweep at high temperatures.

**REFERENCES**


