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Quantization noise upconversion effects in mixer-first direct delta sigma receivers

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Abstract

In this paper we investigate the application of the direct $\Delta\Sigma$ receiver (DDSR) concept in a mixer-first architecture. Specifically, we analyze the degrading effects of quantization noise (Q_n) upconversion on DDSR sensitivity which is a major concern in mixer-first DDSR architecture. We demonstrate that with the chosen approach the mixer-first architecture is suitable for the DDSR despite the potential challenges arising from quantization noise (Q_n) upconversion. A systematic modeling and understanding of Q_n upconversion effects is presented which lead to simple design guidelines. The results demonstrate that a first order low pass Q_n filtering is sufficient in most cases for a mixer-first DDSR implementations. Based on analytical results, we design a transistor-level mixer-first DDSR by merging the functionality of N-path capacitors both as channel select and Q_n filters. Simulations performed in a 28nm CMOS process show a mere 1.5dB degradation from maximum SNDR for the worst case scenarios arising from Q_n upconversion effects, validating the chosen approach.

KEYWORDS:

Quantization noise, N-path filter, $\Delta\Sigma$ modulator, Direct $\Delta\Sigma$ receiver, dynamic range.

1 | INTRODUCTION

Digital-intensive receiver architectures offer relative ease of tunability and scaling from one CMOS generation to next. One such promising architecture is direct $\Delta\Sigma$ receiver (DDSR) (1, 2). The architecture embeds the direct conversion RF front-end as a part of $\Delta\Sigma$ modulator loop filter. In this way, the RF stages perform dual role of low noise amplification/filtering while acting as frequency translating integrator stages. Consequently, total number of stages in receiver are reduced.

As is typical in LNA-first receiver architectures, the linearity of reported DDSRs is dominated by the linearity of the front-end (1, 3). This limitation makes it challenging to approach the dynamic ranges of state-of-the-art traditional delta-sigma adcs (4, 5, 6, 7). One possibility to improve the dynamic range of DDSR is to implement it with generally more linear mixer-first architecture (8). However, as will be explained, mixer-first architecture creates additional challenges on the lower-edge of dynamic range bounded by receiver sensitivity.

The sensitivity of the DDSR is determined mainly by the first stage. The DDSRs published to date include an LNA that relaxes the noise performance requirements of the following circuits. In a mixer-first architecture the LNA is absent and the most significant noise contributor is typically the first baseband amplifier. Applying the DDSR concept in the mixer-first architecture brings four additional noise sources originating from the first feedback DAC. These noise sources are flicker noise, thermal noise, jitter of the clock and upconversion of the spectrally repeating quantization noise. The first three noise sources are present in any

FIGURE 1 Conceptual diagram of mixer-first DDSR with the depiction of quantization noise upconversion path. Dashed lines represent upconverted negative image frequencies while solid lines represent positive frequencies.

sampling circuit and together with the first baseband amplifier will define the receiver baseline noise figure (NF). However, the fourth source of quantization noise in some cases may increase the receiver baseline NF due to the upconversion effects caused by the mixer. Therefore, its effects should be analyzed more strongly.

As depicted in Fig. 1, the quantization noise (Q_n) spectrum present at the output of the DDSR gets upconverted to RF nodes through upconverting mixers in the $\Delta\Sigma$ feedback. As will be detailed in the next section, a non-optimal ratio between quantizer sampling and mixer local-oscillator frequency (f_s/f_{LO}) will result in unsymmetrical upconversion of positive and negative frequencies, consequently increasing the inband input referred noise (9). It is therefore imperative to analyze these effects before implementing a mixer-first DDSR.

In this paper, we will focus on investigating the Q_n upconversion effects on DDSR sensitivity specifically for the more critical case of mixer-first topology. As receiver sensitivity performance defines the lower edge of dynamic range thus reducing the degrading effects of quantization noise on DDSR sensitivity will have a direct impact on receiver dynamic range. On the other hand, the upper-edge of dynamic range bounded by linearity issues will not be the scope of this paper. Systematic understanding and modeling of Q_n upconversion will be presented which lead to simple design equations for selection of DDSR parameters. Further, the results will demonstrate that a simple first order low pass filtering is sufficient in most implementations for an adequate suppression of Q_n . To validate our findings, we design a transistor-level mixer-first DDSR by merging the functionality of N-path capacitors both as channel select and Q_n filter. Simulations performed in a 28nm CMOS technology show a mere 1.5dB degradation from maximum SNDR for the worst case scenarios arising from Q_n upconversion effects.

The organization of this paper is as follows: Section 2 details the Q_n upconversion effects in DDSR's which is followed by modeling of upconverted Q_n in Section 3. Section 4 covers the design details of a mixer-first DDSR. Then based on results from Section 3 and 4, we present a transistor level mixer-first DDSR in Section 5.

2 | QUANTIZATION NOISE UPCONVERSION IN DDSRS

Fig. 2 (c) shows a typical DDSR output spectrum. The inherent noise shaping of $\Delta\Sigma$ converter causes the output Q_n to be low around DC and at multiples of sampling frequency (f_s). Further, the sinc function originating from the zero-order hold functionality of quantizer helps to attenuate the Q_n at higher offsets.

The effect of Q_n upconversion can be comprehended by selecting two different f_{LO} frequencies for upconversion as follows: In the first case, f_{LO} is chosen as $f_s/3$. If f_{LO} is a square wave, higher order odd harmonics will also be upconverted along with fundamental f_{LO} . Fig. 2 (d) shows upconverted DDSR spectrum when $f_{LO} = f_s/3$ where dashed lines represent the Q_n folding from negative frequencies. As can be observed, the upconverted positive and negative frequencies are not symmetric around DC. This causes substantial increase in desired channel Q_n levels where the main contributor for the desired channel Q_n is from the negative frequencies. It can be shown that the maximum impact of upconverted Q_n in the desired RF channel will occur when $f_{LO} = n(f_s/4)$, where n is an odd integer (9). This is because the maxima of upconverted Q_n spectrum from negative frequencies will fall in the desired channel.

In the second case, the degrading effects of Q_n upconversion can be minimized by having $f_{LO} = n(f_s/2)$ as illustrated in Fig. 2 (e). Now the upconverted Q_n is symmetric and has minima at the desired frequency. This is straight forward to achieve by generating f_s from f_{LO} with a fixed ratio as suggested in (10). However, maintaining a specific ratio between f_{LO} and f_s is not always desirable, since the varying f_s will be limited by stability of $\Delta\Sigma$ loop filter in the lower edge and exceedingly high power

FIGURE 2 a) A four stage CIBF mixer-first DDSR model. b) Modeling of H_{mixer} and H_{FB} c) Q_n spectrum at DDSR output y d) Q_n upconversion at $f_{LO} = f_s/3$ e) Q_n upconversion at $f_{LO} = f_s/2$.

consumption on the higher edge. In such a case, a constant f_s will be more easier to implement while f_{LO} will vary across the desired frequency bands. For such a scenario, a practical example can be given for a wideband DDSR implementation targeted for long-term evolution (LTE) bands from 700MHz to 6GHz. The minimum oversampling ratio requirements of the DDSR loop filter may prevent the designer to use 700MHz f_s while on the other hand f_s of 6GHz will lead to excessive power consumption in clock circuits. This will lead to selection of f_s which is neither too high nor too low while f_{LO} will be swept across the reception bands resulting in cases where f_{LO} can be lower or higher than f_s .

Another option is to implement an finite impulse response (FIR) filter in the upconversion path as demonstrated for LNA first DDSR in (1). However, feasibility of an FIR filter implementation still needs to be evaluated for more critical case of mixer-first DDSR with no RF gain. Therefore, in the next section, we provide the required modeling and analysis of upconverted Q_n in mixer-first DDSR. The analysis results lead to design guidelines that reduce the degrading effects of upconverted Q_n .

3 | MODELING OF QUANTIZATION NOISE IN MIXER-FIRST DDSRS

3.1 | Modeling

For the quantitative modeling and analysis of upconverted Q_n , we choose a four stage mixer first DDSR architecture implemented from cascade of integrators in feedback loop filter topology. The selection of a four stage DDSR is taken here as an example and analysis can be easily for other number of DDSR stages. Nevertheless, in next section we will elaborate why the initial choice of four stages is taken.

The chosen DDSR together with its simplified s-domain model is presented in Fig. 2 (b-c). We model upconverted Q_n path with transfer function $H_{FB,upn} = V_{RF}/y$ defined from DDSR output to RF input at n-th harmonic frequency, where n is an odd integer, and noise transfer function $NTF = y/Q_n$. We also define an additional transfer function $H_{FB} = V_{BB}/y$ which will be needed to define the NTF. The rest of the feedback paths do not contain any upconversion and can be modeled in same way

as traditional $\Delta\Sigma$ modulator. Further, the coefficients a_{1-3} and b_{1-3} , described in Fig. 2 (a), represent feedforward and feedback loop filter coefficients, $H_I(s)$ represent integrator transfer function and $H_Q(s)$ represents quantizer transfer function.

For the chosen architecture, the upconverted Q_n rms voltage in $V/\sqrt{Hz}$ at the RF input nodes can be given as:

$$Q_{up} = \sum_{n=1,3,5,7..}^{\infty} H_{FB,upn} \cdot NTF \cdot Q_n, \quad (1)$$

where Q_n represents the maximum value of quantizer rms noise voltage in $V/\sqrt{Hz}$ given by:

$$Q_n = \frac{\Delta}{\sqrt{6f_s}}, \quad (2)$$

where Δ represents the quantizer step size and f_s is the quantizer sampling frequency. Further, the NTF for the presented model can be calculated as:

$$NTF = \frac{1}{1/H_Q + a_1 a_2 a_3 H_{FB} H_I^3 + a_2 a_3 b_1 H_I^3 + a_3 b_2 H_I^2 + b_3 H_I}, \quad (3)$$

Evaluation of NTF requires defining transfer functions H_I , H_{FB} and H_Q . If we assume a non-return-to-zero (NRZ) DAC implementation, $H_Q(s)$ can be modeled with a quantizer gain G_Q and sampling frequency f_s as (10):

$$H_Q(s) = G_Q \frac{1 - e^{-s(1/f_s)}}{s(1/f_s)}, \quad (4)$$

Further, H_I is modeled as a ideal integrator with transfer function $1/s$ while H_{FB} can be calculated based on the modeling of passive N-path mixer non-idealities in (11) as:

$$H_{FB} = \frac{4Z_{BB}g_{m,FB}(Z_{RF} + R_{SW})}{2Z_{RF} + 2R_{SW} + Z_{BB}}, \quad (5)$$

where Z_{BB} represents the input impedance of first baseband transconductor, $g_{m,FB}$ is the effective transconductance of first current steering DAC (IDAC), Z_{RF} is the impedance connected to the RF side of the downconversion mixer and R_{SW} is the mixer switch resistance.

In a similar manner to H_{FB} and following the analysis performed in (11), we can derive the $H_{FB,upn}$ at n-th harmonic frequency of f_{LO} as:

$$H_{FB,upn} = \frac{4\sqrt{2}}{n\pi} \frac{g_{m,FB} Z_{BB,tot}}{(1 + \gamma Z_{BB,tot} Y_{up})} \frac{Z_{RF}}{Z_{RF} + 2R_{SW}}, \quad (6)$$

$$Y_{up} = \sum_{p=-\infty}^{\infty} \frac{2}{(4p+1)^2(Z_{RF} + 2R_{SW})}. \quad (7)$$

Here p is an integer number, $\gamma = 2/\pi^2$ for 25% duty cycle quadrature mixers and $Z_{BB,tot}$ is the parallel combination of baseband input impedance Z_{BB} , impedance of N-path capacitance Z_{CNP} and virtual shunt impedance Z_{SH} representing the power dissipation due to baseband signal upconversion given by (12):

$$Z_{SH} = \left(\sum_{n=3,7,11..}^{\infty} \frac{1}{n^2 Z_{RF}^*(nf_{LO})} + \sum_{n=5,9,13..}^{\infty} \frac{1}{n^2 Z_{RF}(nf_{LO})} \right)^{-1} \quad (8)$$

The upconverted quantization noise Q_{up} will add up directly with the input referred thermal noise of receiver. This essentially means that in order to have minimal effect on overall receiver NF, the Q_{up} must be significantly lower than input referred thermal noise ($N_{thermal}$). Mathematically, we can write:

$$NF = 10 \log_{10} \left(F_{LIN} + \frac{Q_{up}^2}{4kT Z_{RF}} \right) \quad (9)$$

where k is Boltzmann's constant, T is the temperature in Kelvin and F_{LIN} is the receiver noise factor without Q_n contribution. For a minimal impact of Q_{up} on receiver noise figure, $Q_{up}^2/4kT Z_{RF} \ll F_{LIN}$.

FIGURE 3 Comparison between conventional $\Delta\Sigma$ loop filter with no pole splitting and loop filter design for DDSR with pole splitting. (a) Conventional $\Delta\Sigma$ loop filter with no pole splitting and, (b) loop filter design with pole splitting.

3.2 | Evaluation

To quantitatively analyze the effects of upconverted Q_n on receiver NF, we will evaluate the derived equations for some typical receiver specifications. We assume an initial NF = 5dB, constituting from the thermal noise of receiver, and maximum blocker of -10dBm at 10times baseband bandwidth (f_{BW}). While the chosen specs are not linked to any particular communication standard they still approximate what is usually needed. Our target is to analyze in which conditions upconverted quantization degrade the receiver NF. This evaluation is done by taking an example DDSR implementation which is based on the DDSR design principles established in our previous work (10). There we have highlighted that traditional design methods of $\Delta\Sigma$ modulators are not optimal for DDSR design. Some of the main design differences that will be implemented in this evaluation are highlighted below:

- In a conventional $\Delta\Sigma$ loop filter design, STF and NTF are linked to each other. Fig. 3 (a) shows the output spectrum of a conventional first order $\Delta\Sigma$ modulator having the required channel select filtering bandwidth of f_{BW} . When this $\Delta\Sigma$ modulator is used as a DDSR, the target is to reduce the in-channel Q_n as much as possible. This can be done by pushing the NTF and STF cutoff frequency (f_C) higher. A very high f_C provides maximum quantization noise shaping but attains poor blocker attenuation. On the other hand, good blocker attenuation requires a very low f_C . Therefore, selection of f_C is a compromise between in-channel Q_n reduction and blocker attenuation. The compromise can be avoided in higher order $\Delta\Sigma$ modulators by splitting channel select filtering (f_{BW}) and noise shaping pole (f_{NSP}) frequencies. As depicted in Fig. 3 (b), the STF and NTF poles are split into f_{BW} and f_{NSP} where a lower f_{BW} helps with increased blocker suppression and a higher f_{NSP} yields minimal in-channel quantization noise. In addition, separating these frequencies far allows us to independently design two filters with minimal impact on each other. Another key point to note here is that the even though at first glance it may seem that stages with f_{BW} poles are only for channel selection and stages with f_{NSP} poles for noise shaping, all stages contribute in the noise shaping.
- DDSR should be designed with only minimum amount of gain to suppress the noise contribution of later stages. This is because in practical implementations ideal filtering of blockers is not possible. Filtering stages will always have a limited filter roll-off. This means that a higher gain will also increase the near-band blocker power and therefore will reduce the out-of-band linearity. For example, a 20dB gain in first stage of DDSR will suppress about 10times the contribution from later stages noise and unless later stages are extremely noisy, a gain of 15-20dB should suffice in most practical cases.

Once the required value of gain has been chosen, the required number of channel select filtering stages (filter order) can be selected based on the target level of blocker attenuation at a certain offset. The required level of blocker attenuation at a certain offset can be found as (10):

$$G_{blk} = P_{max} - P_{blk,max} \quad (10)$$

where P_{max} defines the maximum internal node power of designed amplifier while the $P_{blk,max}$ is the maximum blocker power. Assuming, $P_{max} = -20\text{dBm}$, as it is practically achievable in used 28nm FDSOI technology, G_{blk} can be calculated as -10dB. Therefore, if we target a 20dB inband gain then first order filtering with 20dB/decade attenuation will not be sufficient to reduce

FIGURE 4 Upconverted quantization contribution from different LO harmonics at different f_{BW}/f_S ratios. $f_{NSP}/f_S = 0.1$, $\Delta = 1V$, $G = 20dB$, and $f_{LO}/f_S = 3/4$.

FIGURE 5 Upconverted quantization contribution from different LO harmonics at different f_{LO}/f_S ratios. $\Delta = 1V$, $G = 20dB$, $f_{BW}/f_S = 0.02$ and $f_{NSP}/f_S = 0.1$.

the blocker gain to $-10dB$ at $10f_{BW}$. Consequently, we select two stage filtering for channel-select filtering for the evaluated DDSR.

The total number of required integration stages depends on the selected sampling rate, number of quantizer bits (more specifically the Δ) and the loop filter order. As a trade-off between quantizer complexity, number of stages and sampling rate, we have chosen to add two stages that will be mainly responsible for the quantization noise shaping, bringing the total number of stages to 4.

After the selection of number of stages, next step is to 2nd order filtering profiles. We choose here Butterworth filter coefficients as they have minimal peaking in overall STF.

As multiple parameters can affect Q_{up} , we will focus on one parameter at a time while keeping others fixed at certain value. Mainly, we will analyze the effects of baseband bandwidth to sampling frequency ratio (f_{BW}/f_S), local oscillator to sampling frequency ratio (f_{LO}/f_S), quantizer step size (Δ), N-path capacitance (C_{NP}), and receiver gain (G). The results will then be validated with behavioral simulations.

In Fig. 4, the Q_{up} from different LO harmonics is plotted vs. f_{BW}/f_S while keeping f_S constant. One can observe a higher Q_{up} for higher f_{BW}/f_S ratios. This behavior can be explained as follows: The f_{BW} is controlled by the first two stage poles, created by C_{NP} and C_2 , forming a second order filter. C_{NP} comes directly in Q_n upconversion path as a first order filter and is therefore the main contributor for the behavior in Fig. 4. A smaller C_{NP} results in upconversion of wider band of Q_n consequently increasing inband Q_{up} . Generally, designer does not have freedom to control C_{NP} value as it is dictated by required f_{BW} of receiver. Nevertheless, regardless of C_{NP} value, it helps in both channel select and Q_{up} filtering which is beneficial from the performance point-of-view.

Fig. 4 also elaborate a key design difference between a DDSR and a typical $\Delta\Sigma$ ADC. As is the case in typical $\Delta\Sigma$ ADC, choosing $f_{BW} = f_{NSP}$, where f_{NSP} is the NTF pole frequency, will result in substantial increase in Q_{up} . Therefore, for an optimum receiver sensitivity performance, f_{NSP} should be chosen much larger than f_{BW} . This is also beneficial in ease of implementation as we can independently design f_{BW} and f_{NSP} loop filters.

FIGURE 6 Effect of positive (black) and negative (gray) sides of upconverted spectrum at two different f_{LO}/f_S ratios. $f_{LO}/f_S = 1/4$ ratio leads to higher Q_{up} . $\Delta = 1V$, $G = 20dB$, $f_{BW}/f_S = 0.01$ and $f_{NSP}/f_S = 0.1$.

FIGURE 7 Upconverted quantization contribution for different quantizer step sizes. $f_{LO}/f_S = 3/4$, $\Delta = 1$, $G = 20dB$, $f_{BW}/f_S = 0.02$ and $f_{NSP}/f_S = 0.1$.

FIGURE 8 Upconverted quantization contribution for different values of receiver gain. $f_{LO}/f_S = 3/4$, $\Delta = 1V$, $f_{BW}/f_S = 0.01$ and $f_{NSP}/f_S = 0.1$.

In Fig. 5, Q_{up} from different LO harmonics is plotted vs. f_{LO}/f_S while keeping f_S constant. As expected, the Q_{up} follows a zig-zag behavior, having much higher Q_{up} for the worst case frequencies of $f_{LO} = n(f_S/4)$. One can also observe that Q_{up} is very high for $f_{LO}/f_S = 1/4$. This can be explained through Fig. 6 where we plot the positive and negative sides of Q_{up} at two different f_{LO}/f_S ratios. One can observe that even after C_{NP} filtering effect, the sum of Q_{up} from positive and negative sides of spectrum is higher for $f_{LO}/f_S = 1/4$ than $f_{LO}/f_S = 3/4$ and therefore, will degrade the receiver NF more severely.

In Fig. 7, the Q_{up} from different LO harmonics is plotted for different values of quantizer step size Δ . One can observe that Q_{up} is a weak function of Δ . This is expected as the effect of C_{NP} already filters out huge portion of Q_n . However, in order to have minimum effect on Q_{up} , Δ should be chosen as low as possible.

In Fig. 8, the Q_{up} from different LO harmonics is plotted at different values of receiver gain. Results show that higher values of receiver gain are beneficial in terms of reduced Q_{up} . However, as we detailed in (10), only a minimum amount of gain should

be applied in DDSR's which is deemed sufficient to reduce the noise contribution from later stages. Lower gain will improve the large signal performance of receiver. Therefore, selection of gain is a compromise between Q_{up} and receiver large signal linearity and should be chosen to a minimum value which has acceptable noise performance.

From the above results we can establish following design guidelines for mixer-first DDSR:

- It is a good idea to limit the bandwidth of mixer nodes to f_{BW} where f_{BW} should be much lesser than f_{NSP} and f_S . This is in contrast to typical $\Delta\Sigma$ ADC design where $f_{BW} = f_{NSP}$. Selecting $f_{NSP} \gg f_{BW}$ will also allow independent design of f_{BW} and f_{NSP} loop filters.
- Among the worst case $f_{LO} = n(f_S/4)$ frequencies, $f_{LO}/f_S < 1/2$ are most problematic. First order C_{NP} filtering may not be enough to filter upconverted Q_n for such ratios.
- Selection of higher number of quantizer bits is beneficial for reduced upconverted Q_n but is not a strong function.
- In contrast to a typical $\Delta\Sigma$ ADC design, selecting a unity gain loop filter is not beneficial in DDSR. Gain should be high for reduced Q_{up} . From our previous design experience 15-20dB gain should suffice in most cases.

4 | MIXER FIRST DDSR DESIGN

Our target is to design a mixer-first DDSR with high dynamic range and with little to no impact on dynamic range from Q_n upconversion effects. In other words, the lower edge of the receiver dynamic range should be bounded mainly by input referred thermal noise of first baseband amplifier and current steering DAC.

4.1 | Loop filter order

To achieve the above design criteria, we start with initial design targets of receiver from 0.7-2.7GHz operating frequency, baseband bandwidth of 10MHz and a maximum acceptable blocker power of -10dBm at 100MHz offset. Though the initial design targets are not linked to any particular standard, they lie within the range of what is usually needed in mobile communications. We will also choose a receiver gain of 15dB as it is sufficient to reduce the noise contribution from later stages in most cases. From the chosen gain and target blocker attenuation requirement, minimum required attenuation for the blocker from equation 10 comes out to be -10dB. This will lead to a requirement of second order channel-select filtering.

The next step is to design the DDSR loop filter to meet the design targets. As explained in Section 3.2, we will partition loop filter poles into channel select filtering poles and noise shaping poles at frequencies f_{BW} and f_{NSP} respectively. The number of channel-select filtering poles have already been calculated as two while the number of noise shaping poles need to be calculated. The noise shaping poles will be mainly responsible for shaping the Q_n in high-pass response such that little to no Q_n remains inside the desired channel. The total number of required noise shaping poles mainly depend on the selected sampling rate, number of quantizer bits (more specifically the Δ) and the loop filter order. The required number of noise shaping pole stages (N) can be calculated by matching thermal and quantization noise densities at f_{BW} and is given as (10):

$$N = \frac{\log_n\left(\frac{\Delta^2}{6f_S k T G_{RX} F_{LIN}}\right)}{2\log_n\left(\frac{f_{NSP}}{f_{BW}}\right)} \quad (11)$$

where G_{RX} is the receiver power gain and F_{LIN} is the noise factor of the receiver excluding Q_n . The calculation of N requires initial values for variables such as Δ , f_S , f_{NSP} and, F_{LIN} . Below we choose some practical values of these variable with an explanation of choosing criteria.

First, the quantizer step size Δ is dependent on the quantizer number of bits and maximum input swing range of the quantizer. A single bit quantizer is simpler to design but is quite sensitive to sampling clock nonidealities such as jitter. On the other hand, higher number of quantizer bits generally result in increased power and circuit complexity. Therefore, for the implemented mixer-first DDSR, we choose a 2bit quantizer as it provides a good compromise between lower complexity and resilience against sampling clock non-idealities. The chosen quantizer input swing range should be selected so that it will not limit the maximum input signal level, meaning a minimum single-ended full-swing of P_{max} of -20dBm or 32mV from Section 3.2. To ensure that the quantizer input signal swing is not the limiting factor in determining the receiver linearity, we select a quantizer input swing range (V_{FS}) of 100mV. Therefore, Δ will become $\Delta = V_{FS}/(2^2 - 1) = 33.3mV$

Second, the f_s value is limited by stability of $\Delta\Sigma$ loop filter in the lower end and exceedingly high power consumption on the higher end. Therefore, we choose a central value $f_s = 1.5\text{GHz}$ across the required receiver band of $0.7\text{-}2.7\text{GHz}$. Third, the noise shaping pole frequency f_{NSP} affects the in-band attenuation of quantization noise. To maximize this attenuation, it is beneficial to position f_{NSP} as high as possible. The limiting factor is f_s as placing f_{NSP} closer to f_s will increase the risk of instability. A practical value extracted from the simulations will be $f_s > 4f_{\text{NSP}}$ (10). We choose $f_{\text{NSP}} = 100\text{MHz}$ as safety margin which is well below $f_s/4$. Fourth, the F_{LIN} is selected based on the target NF of the receiver. Assuming a 5dB NF target, F_{LIN} will become 3.16.

The above chosen values lead to $N \approx 2.75$. This shows that we either need three noise shaping pole stages with $f_{\text{NSP}} = 100\text{MHz}$ or two noise shaping pole stages with a higher f_{NSP} . The second option is chosen to reduce the number of stages. For $N = 2$, new f_{NSP} will become (10):

$$f_{\text{NSP}} = f_{\text{BW}} \left(\frac{\Delta^2}{6f_s k T G_{\text{RX}} F_{\text{LIN}}} \right)^{\frac{1}{2N}} \quad (12)$$

leading to $f_{\text{NSP}} = 235\text{MHz}$ which is still lesser than our maximum practical limit of $f_s/4$. This leads to total of four stages in loop filter where first two stages will be utilized for channel-select filtering at f_{BW} while the later two stages will be mainly responsible for shaping of quantization noise with higher f_{NSP} . As f_{NSP} and f_{BW} quite further apart in frequency, therefore, the channel select filtering stages and noise shaping poles stages can be designed independently without much effect on each other response. We will also target minimal peaking in the STF and therefore will design the loop filter STF with two second-order butterworth responses in series.

4.2 | Loop filter implementation

Fig. 2 c) presents the block level diagram of four stage DDSR architecture. The architecture differs from conventional $\Delta\Sigma$ loop filter due to the presence of first frequency translation integration stage. The frequency translating integrator stage, which is most important in shaping Q_{up} , consists of passive quadrature downconversion mixers with 25% dutycycle together with C_{NP} as N-path capacitor. The capacitor C_{NP} provides dual roles of channel select and quantization noise filtering. The frequency translating stage can modeled with a transfer function $H_{\text{mixer}} = V_{\text{BB}}/V_{\text{RF}}$ defined from RF inputs to first baseband stage input. The first feedback path will also be influenced by the presence of frequency translating integrator stage and is therefore modeled with transfer function $H_{\text{FB}} = V_{\text{BB}}/y$ defined from DDSR output to first BB stage input. Using the N-path passive mixer model presented in (12), H_{mixer} can be derived as:

$$H_{\text{mixer}} = \frac{\pi}{2\sqrt{2}} \frac{2\gamma Z_{C,NP} || Z_{SH} || 2\gamma Z_{BB}}{2\gamma Z_{C,NP} || Z_{SH} || 2\gamma Z_{BB} + R_{SW} + Z_{RF}}, \quad (13)$$

The feedback transfer function H_{FB} can be given as:

$$H_{\text{FB}} = \frac{2Z_{BB}g_{m,FB}(Z_{RF} + R_{SW})}{2Z_{RF} + 2R_{SW} + Z_{BB}}, \quad (14)$$

where $g_{m,FB}$ represented the transconductance of first stage feedback DAC. Given H_{FB} and H_{mixer} , we can find the signal transfer function (STF) for the mixer-first DDSR as:

$$\frac{a_1 a_2 a_3 H_{\text{mixer}} H_I^3}{1/H_Q + a_1 a_2 a_3 H_{\text{FB}} H_I^3 + a_2 a_3 b_1 H_I^3 + a_3 b_2 H_I^2 + b_3 H_I}, \quad (15)$$

For the two second order butterworth filters in series, initial feedforward and feedback coefficients are thus $a_1 = 1$, $b_1 = 1$, $a_2 = 1$, $b_2 = \sqrt{2}$, $a_3 = 1$, $b_3 = 1$, $a_4 = 1$, and $b_4 = \sqrt{2}$ (13). These coefficients are for unity gain and will need to be first scaled to required receiver voltage gain G_V . As the first frequency translating integrator stage is passive in nature, it will provide a loss. Therefore, gain from later stages should be larger than required G_V in order to achieve an overall gain of G_V from receiver. We choose to provide all gain from first baseband amplifier because having gain in later stages does not benefit in terms of receiver NF. The value of second stage gain G_2 can then be found as $G_2 = G_V/G_1$. Stages three and four only contribute in noise shaping and therefore are designed with unity gain. The actual gain from first frequency translating stage G_1 , for the impedance matched condition, can be found by substituting,

$$Z_{BB} \approx \frac{Z_{SH}(Z_{RF} - R_{SW})}{2\gamma(Z_{SH} - Z_{RF} + R_{SW})} \quad (16)$$

in Eq. 13 for H_{mixer} . The value of above Z_{BB} ensures impedance matches to 50Ω source at mixer RF inputs. Using this value of G_1 , the initial feedforward and feedback loop filter coefficients are now scaled with gain and are provided in table 1. The scaled coefficients in table 1 result after dynamic voltage scaling and referring all coefficients to baseband channel-select filter bandwidth $f_{\text{BW}} = f_{\text{RFBW}}/2$ such that noise shaping filter cutoff frequency $f_{\text{NSP}} = \alpha f_{\text{BW}}$. The missing a_1 feedforward coefficient is defined through H_{mixer} while the first feedback coefficient b_1 will be embedded as part of H_{FB} when calculating C_{NP} .

Using Eq.13, we can also find the value of N-path capacitor C_{NP} and is given as:

$$C_{\text{NP}} \approx b_1 \frac{2\gamma[1 + (Z_{\text{RF}} + R_{\text{SW}})(1/Z_{\text{SH}} + 1/2\gamma Z_{\text{BB}})]}{2\pi f_{\text{BW}}(Z_{\text{RF}} + R_{\text{SW}})} \quad (17)$$

The function of first feedback is not only to provide DDSR feedback for quantization noise shaping but also to provide required impedance matching in mixer-first DDSR implementation. This is done by achieving first baseband stage input impedance equal to Z_{BB} in Eq. 13 by tuning $g_{\text{m,FB}}$ in feedback path. The required value of $g_{\text{m,FB}}$ to produce input impedance match, can be derived as:

$$g_{\text{m,FB}} \approx \frac{2\gamma(Z_{\text{SH}} - Z_{\text{RF}} + R_{\text{SW}})}{Z_{\text{SH}}(Z_{\text{RF}} - R_{\text{SW}})G_0G_1G_2G_3} \quad (18)$$

where G_3 and G_4 represents gain from stages 3 and 4. Rest of feedback transconductances and integrating capacitor values can be found in traditional way of CIFB loop filter implementation.

Based on above design equations, we will now design a transistor level mixer-first DDSR in next section. The designed circuit will also validate our theoretical findings presented in section 3.

5 | IMPLEMENTATION AND SIMULATED RESULTS

The proposed mixer first DDSR was evaluated in a 28nm fully-depleted silicon-on-insulator (FD-SOI) process through noise transient and steady state analysis. The schematic of implemented circuit is shown in Figure 9. The DDSR is designed for a configurable band of 0.7-2.7GHz with a BB bandwidth f_{BW} of 10MHz.

5.1 | Frequency translational integrator

The first stage of DDSR consisting 25% duty cycle passive quadrature passive mixers, N-path capacitance C_{NP} , source resistance R_{S} and the first feedback current steering DAC (IDAC) form the frequency translational integrator stage. Transistors with a large aspect-ratio of $24/0.03\mu\text{m}$ were implemented in passive mixers. This ensures a small switch resistance of approximately 10Ω for better attenuation at far away offsets from f_{LO} . Value of C_{NP} is set to meet the baseband bandwidth requirements of 10MHz.

5.2 | Baseband transconductors

To maximize the input and output swing range of baseband amplifiers, push-pull single stage OTA structures were implemented as shown in Figure 10. As the first baseband amplifiers noise constitutes a major role in overall receiver NF, a high transistor transconductance was chosen to implement the first amplification stage. On the other hand, last two stages of baseband noise requirements are relaxed by preceding voltage gain and hence had transconductance values half of first baseband stage. The requirement of last two stages transconductance was also effected by the slew rate and loading requirements of these stages.

5.3 | Current steering DAC's and quantizer

Figure 10 shows the implemented 2-bit current-steering DAC's using thermometer weighting and push-pull current steering cells. The dimensions transistors in current-steering DAC's were chosen for lower flicker noise while having higher output impedance compared to baseband amplifier inputs. A two bit quantizer was chosen as it provides a good compromise between lower complexity and resilience against sampling clock non-idealities. The implementation was done with behavioral modeling to have the flexibility to test Q_n upconversion effects in worst-case scenarios. A clock delay of $t_s/10$ was added in the quantizer and feedback DAC path to model the excess loop delay in the feedback path. Here t_s is the time period of the sampling frequency f_s .

FIGURE 9 Implemented mixer-first DDSR

FIGURE 10 Implemented circuits for a) current steering DAC b) baseband amplifiers. The transistor dimensions are for first feedback IDAC and first baseband amplifier. Dimensions of later IDACs are four times smaller while two times smaller for baseband amplifiers.

5.4 | Simulated Results

The spectrum of the DDSR output bit stream through noise-transient simulations, with both thermal and quantization noise included, is shown in Fig. 11. DDSR functionality is observed through following. First, the desired in-band signal is amplified with around 15dB of RX gain. Second, the blocker is attenuated by the channel select filtering response and third, the Q_n is shaped by the DDSR feedback loop such that there is little in-band Q_n left.

In Fig. 12, DDSR SNDR versus input signal power is plotted. the RX achieves a maximum SNDR of 60dB at P_{IN} of -33dBm. At low signal powers, the difference between ideal and simulated SNDRs is approximately equal to RX NF.

In Fig.13, the simulated SNDR vs. f_{LO} is presented for different standard deviations of sampling clock jitter. We keep the sampling frequency constant at 1.5GHz which means that across 0.5-2.7GHz f_{LO} sweep, there will be worst case f_{LO}/f_S ratios. Nevertheless, as explained in Section 3, N-path capacitor C_{NP} will filter out majority of upconverted Q_n , resulting in quite small degradation in maximum SNDR for different f_{LO}/f_S ratios. As expected, a mere 1.5dB of maximum degradation in the receiver SNDR is observed from the upconverted Q_n even for the worst case f_{LO}/f_S ratios. As maximum SNDR occurs when any non-linear products are lower than thermal noise floor of the receiver, one can establish the receiver NF will also follow the same behavior at different f_{LO}/f_S ratios validating the reduced Q_{up} . The impact of f_S jitter lowers the overall SNDR. Nevertheless, the maximum SNDR degradation remains about the same across different f_{LO}/f_S ratios.

Table 2 presents a the performance comparison of implemented mixer-first DDSR. We are able to achieve a much higher SNDR of 60dB in comparison to other published DDSRs. It was observed in simulations that the peak SNDR was limited by the non-linearity arising from IDAC's. The voltage swing at the input of first baseband amplifier (also connected to first IDAC output) was causing the IDAC current sources to enter in non-linear region. Nevertheless, we estimate that implementing the IDACs with cascaded current sources will improve the IDAC linearity as there will be smaller voltage swing across the main transistor in current source. The simulated NF of the designed mixer-first receiver is higher than other compared works mainly due to the input referred thermal noise of the first baseband amplifiers and first current steering DAC. Nevertheless, as can be established from Fig. 13, the variation of NF from Q_n upconversion effects, across different f_{LO}/f_S , is not more than 1.5dB validating the presented approach.

FIGURE 11 Output spectrum at $f_{LO} = f_S = 1.5\text{GHz}$, Signal power $P_{in} = -42\text{dBm}@f_{LO}+1.83\text{MHz}$, Blocker power $P_{blk} = -42\text{dBm}@f_{LO}+70\text{MHz}$ and $f_{BW} = 10\text{MHz}$.

6 | CONCLUSION

Configurable wideband receiver solutions for emerging wireless standards require digital intensive architectures such as the direct $\Delta\Sigma$ receiver (DDSR). In this paper, we have investigated the degrading effects of upconverted quantization noise (Q_{up}) on a mixer-first DDSR sensitivity. This is a major concern in mixer-first DDSR as the Q_{up} can severely degrade receiver sensitivity. Systematic modeling and thorough analysis of Q_{up} lead to simple design guidelines for reduced Q_{up} and demonstrate that first order low pass filtering is sufficient in most cases to suppress the degrading effect of Q_{up} . To validate our findings we implemented a transistor-level mixer-first DDSR by utilizing N-path filtering capacitor with dual role of channel select and Q_n filtering. Thanks to the presented design guidelines, the results demonstrate a mere 1.5dB degradation in receiver peak SNDR even for the worst case f_{LO}/f_S ratios.

FIGURE 12 SNDR versus input power sweep.

FIGURE 13 SNDR versus f_{LO} at different f_s clock jitter standard deviations (σ). $f_s = 1/T_s = 1.5\text{GHz}$ and $P_{in} = -35\text{dBm}$. As desired, minimal impact on receiver SNDR is observed for arbitrary ratios of f_{LO}/f_s .

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TABLE 1 Loop-filter coefficients

Coefficient	a_2	a_3	a_4	b_1	b_2	b_3	b_4
Initial	$\frac{G_V}{G_1}$	1	1	1	$\sqrt{2}$	1	$\sqrt{2}$
Scaled	$\sqrt{2} \frac{G_V}{G_1}$	α	α	$\frac{1}{\sqrt{2}}$	$\sqrt{2}$	$\frac{1}{\alpha\sqrt{2}}$	$\frac{\sqrt{2}}{\alpha}$

TABLE 2 Performance summary and Comparison

	This work ⁽²⁾	(14)	(3)
Frequency (GHz)	0.7-2.7	0.6-3	0.7-2.7
Gain (dB)	15	50	-
Noise Figure (dB)	8.5	2.4-3.5	5.9-8.8
Blocker NF ⁽¹⁾ (dB)	11.5	-	-
Peak SNDR (dB)	60	49	43
f_{BW} (MHz)	10	10	7.5
P_d (mW)@ V_{DD} (V)	35+15@1 ⁽³⁾	35.5-53.5@1.2	90@1.1
Architecture	Mixer first	LNTA first	LNA first
Process	28nm FDSOI	65nm CMOS	40nm CMOS

1) -10dBm blocker at 60MHz offset 2) Simulated response 3) Estimated LO power consumption based on our previously measured DDSR chip is about 15mA.

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