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Published in:
IEEE Systems Journal

DOI:
10.1109/JSYST.2019.2923289

E-pub ahead of print: 19/07/2019

Document Version
Peer reviewed version

Please cite the original version:
Rostami, A., Jalilian, A., Zabihi, S., Olamaei, J., & Pouresmaeil, E. (2019). Islanding Detection of Distributed Generation Based on Parallel Inductive Impedance Switching. IEEE Systems Journal. https://doi.org/10.1109/JSYST.2019.2923289

Islanding Detection of Distributed Generation Based on Parallel Inductive Impedance Switching

Ali Rostami, Amin Jalilian, Sasan Zabihi, Javad Olamaei, *Senior Member, IEEE*, and Edris Pouresmaeil, *Senior Member, IEEE*

***Abstract*--The paper deals with a new islanding detection method based on parallel inductive impedance (PII) switching at distributed generation (DG) connection point, and monitoring the rate of change of voltage (dv/dt) at DG output. In the proposed approach, switching the PII causes variation in the dv/dt. This variation is very small in the case that DG operates in parallel with the main grid, whereas the changes will be very large during the occurrence of islanding. Therefore, the dv/dt is employed to identify both the islanding and non-islanding situations; however, to better analyze the dv/dt changes, the Fast Fourier Transform (FFT) is employed to process the variation of the dv/dt. To select the type of inserted impedance, the effect of switching various impedance types on the *FFT(dv/dt)* is thoroughly analyzed. It is demonstrated that the purely inductive impedance has better performance than other impedance types. The performance of the proposed method is examined through comprehensive simulation studies in MATLAB. The simulation results indicate that the proposed method retains its efficiency for both inverters- and synchronous-based DGs. Moreover, the proposed method not only has a substantial influence on the reduction of disturbances due to the small amount of PII, but it also eliminates the non-detection zone entirely in comparison with other available methods.**

***Index Terms*-- Islanding, parallel inductive impedance switching, fast Fourier transform, the rate of change of voltage.**

I. Introduction

THE inclusion of DGs in power systems, apart from its advantages (e.g., higher reliability and improved power quality) has some drawbacks, such as inadvertent islanding. Islanding occurs when the power system loads are only fed by DG units while the main grid is disconnected. Islanding operation has some hazards and causes several technical problems, e.g., line workers safety issues, unstable voltage, and frequency, and adversely affects the pre-designed protection scheme. According to the above-mentioned hazards of islanding, IEEE 1547 standard emphasizes that it is very crucial to detect the islanding and disconnect the DG units from the main network within two seconds [1], [2]. Islanding detection methods proposed by researchers are generally divided into two main groups, namely remote methods and local methods. Remote methods work based on the communication between DG units and the main network, and are not affected by power match conditions; however, their application is quite uneconomical. Local methods can be classified as passive, active, and hybrid methods [2]. In the following, some methods in each group of the local schemes have been presented, and their drawbacks are also explained to clarity the backgrounds and the innovations of the work.

Passive methods are based on the measurement of changes in the magnitude of various electrical parameters at the point of common coupling (PCC), comparing the measured values with their corresponding threshold values, and finally detecting the occurrence or non-occurrence of islanding. These methods do not have any negative impact on the normal operation of the power system. However, the major drawback of such methods is their inability to detect a perfect match or minor mismatch zones of active and reactive power. Frequency-based and voltage-based methods in [3]-[5] have a non-detectable zone in the case of perfect match and minor mismatch of the active and reactive power. The proposed rate of change of reactive power method in [6] fails for conditions that the power system works at unit power factor or close to it. In fact, a significant value of reactive power is required for its accurate performance. The rate of change of sequence components of currents method may send false tripping command during a three-phase fault to ground [7]. The possibility of false islanding detection during a perfect power match is a drawback of the methods presented in [8-9]. Some of the other passive methods include the rate of change of exciter voltage over reactive power at DG-side, a derivative of the equivalent resistance seen from the DG terminal with respect to angular frequency, inverse hyperbolic secant function, and feature extraction of frequency [10]-[13].

Active methods function according to the reaction of power systems to the disturbance, which changes various electrical parameters of the power system. Therefore, by calculating the extent of changes in the magnitude of electrical parameters with respect to their specified threshold values, islanding or non-islanding can be detected. This method has a greater reliability level and an accurate performance compared to passive methods; however, it reduces the power quality. Major disturbance, long detection time, and inability to distinguish between the islanding and transient events in case of heavy induction loading are some of the disadvantages of active and reactive power compensation method in [14]. Reactive power control method proposed in [15] suffers from long detection

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time in small power mismatches and not being applicable to different types of DGs. The procedure presented in [16] can only be adopted for inverter-based DGs. Load changes in the normal operating condition of the power system may cause interference with the variable impedance insertion method [17]. Some of the other active methods include the active ROCOF relay, voltage harmonic distortion positive feedback [18], [19].

- Hybrid methods use a combination of passive and active methods. For the undetectable zone of the passive methods, an active method is adopted as a complementary extension. Long detection time in comparison with some previously introduced methods that can cause nuisance tripping during some transient events, leading to a remarkable change in the active power of the system are some drawbacks about the average rate of voltage change and real power shift method in [20]. Great disturbance due to switching the large R-L load and interference with load changing in the normal operating of the power system are some drawbacks of the proposed load connecting strategy in [21]. Also, in the capacitor connection strategy, the ROCOV and ROCORP parameters will suffer from appropriate determining the capacitor capacity and thresholds of the selected passive parameters [23]. The introduced method in [24] that uses the breaker switching at DG output, can raise some technical problems such as instability of the DG unit. Meanwhile, its implementation is limited to synchronous-based DG units. The load shedding scheme is the other hybrid method introduced in [25].

This paper presents an islanding detection method based on *FFT(dv/dt)* and PII switching strategy. When the islanding cannot be detected through only *FFT(dv/dt)*, the PII switching is implemented to identify both the islanding and non-islanding situations. In the proposed approach, the parallel inductive impedance switching results in variation in the *FFT(dv/dt)*. The variations of *FFT(dv/dt)* are very small in non-islanding condition; however, its changes will be very large in islanding condition. Therefore, islanding and non-islanding can be easily discriminated by the *FFT(dv/dt)*.

The rest of this paper is organized into three sections. Following the introduction, the general schematic diagram of the proposed model will be introduced in Section II and analyzed in details. Moreover, simulation results have been performed to demonstrate the efficiency and applicability of the developed detection method in Section III. Finally, the conclusions are drawn in Section IV.

II. The Proposed Methodology

The configuration is given in Fig. 1 is considered to investigate the operation principle of the proposed method. As it is shown, a DG unit, either synchronous or inverter-based, is connected to the PCC through a DG breaker. A local load fed at PCC bus and a purely inductive impedance are connected in parallel with the PCC via a dedicated breaker. The PCC voltage is employed as the input of the proposed algorithm.

A. Operational Principle of the Proposed Scheme

Voltage fluctuations caused by switching events is one of the most significant features of the transient changes in the power systems. Therefore, in this paper, it is suggested to utilize impedance switching as an active method to detect DGs islanding. For this purpose, to identify the islanding condition in the proposed scheme, the PII breaker is closed and then immediately has been opened. The switching of the PII at the PCC causes abrupt variations in the electrical parameters of the power system, particularly in the voltage signal. These transient changes are remarkable during the transition to islanded mode, whereas their values are small during normal power system operation.

In fact, during grid-tied mode, the voltage at the PCC is defined by the main grid, and the magnitude of the changes depend on the automatic voltage regulators of the main network. On the other hand, during islanding mode, the magnitude of the PCC voltage is determined by the DGs voltage regulatory mechanism and its dynamic response is irrespective of the DGs type. As a result, during both operating modes, the PCC voltage fluctuations can be used as an effective means to detect islanding and non-islanding events. To demonstrate the differences between the magnitude of the *FFT(dv/dt)* for both operating modes, a typical dynamic variation of the *FFT(dv/dt)* during PII switching is shown in Fig. 2. It can be inferred that because of PII switching at the PCC bus, the maximum magnitude of the *FFT(dv/dt)* is much larger during islanding mode than the grid-tied mode. Hence, As illustrated in Fig. 1, to apply the proposed strategy, regardless of the DGs type, an inductive impedance is added to the PPC bus of the system, and under the certain condition, it is switched on and then immediately off. Then, by monitoring the changes in the voltage at DG output condition are detected. So, the performance of the proposed method is not dependant on the type of DGs, inverter- or synchronous-based DGs; therefore, the operational performance of the proposed scheme is independent of the DG type, and it will retain its appropriate performance while any kind of synchronous DG, as well as inverter-based DGs is connected .

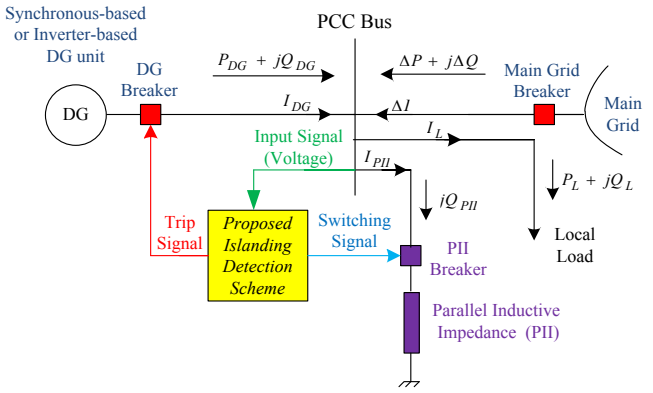

Fig. 1. Schematic diagram of the typical power system equipped with the proposed islanding detection scheme.

B. Sensitivity Analysis for the Inductive Impedance Selection

As mentioned, to identify the islanding condition in the proposed method an impedance is switched on and off at the PCC. In this section, the effect of switching impedances variations, e.g., resistive-inductive and resistive-capacitive

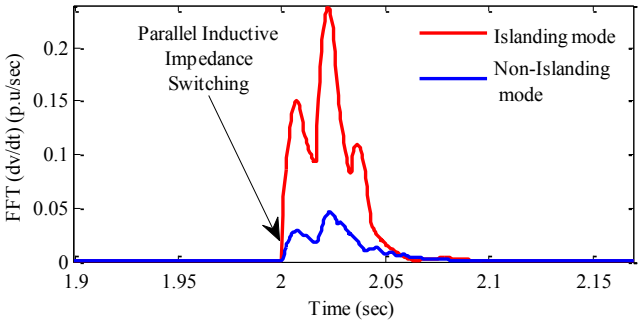

Fig. 2. Typical dynamic variations of the *FFT(dv/dt)* during PII switching for both islanding and non-islanding modes.

with various power factors, purely inductive and purely resistive on the value of the FFT(dv/dt) are evaluated. For this purpose, a set of simulation studies have been carried out on the system depicted in Fig. 3. In Fig. 3, CB3 is opened, so both DGs supply connected loads to the PCC at the islanded operating condition. A 100 kVA impedance with various inductive-capacitive characteristics is selected and simulated. The power factor is gradually changed throughout the study to obtain various types of impedance. Tests are carried out for both islanding conditions with various power mismatches, and also under normal power system operation.

As it is well known and reported in different references such as [30], the passive parameters of islanding detection methods are not affected by different values of the X/R ratio. However, various amounts of the X/R ratio can influence the performance of the active islanding detection methods. Hence, to indicate the effects of the X/R ratio on the changes in *FFT(dv/dt)* during applying the active part of the proposed method (PII switching), a set of simulations studies including various X/R ratios in the range between 0.5 to 10 have been done. The obtained results are shown in Fig. 4. As it is revealed, variation in *FFT(dv/dt)* parameter following the 100 kvar PII switching has not been affected by the value of X/R ratio, and for all values of X/R ratio, the *FFT(dv/dt)* changes is almost similar. In the other word, there is no considerable difference between changes in *FFT(dv/dt)* during the 100 kvar PII switching in the presence of various X/R ratios.

The value of the PII is selected at the lowest possible value that can detect the islanding/non-islanding conditions, so that, it is very smaller than reactive power of the power system loads. Hence, given that the X/R ratio is the ratio of the power system reactance to the resistance, switching the proposed PII does not create the remarkable change in reactance of the power system, as well as the X/R ratio.

Maximum magnitude changes of the *FFT(dv/dt)* after impedance switching for islanded and grid-connected modes are shown in Fig. 5 and Fig. 6, respectively. As Figs. 5 and 6 illustrate, in both modes of operation, the *FFT(dv/dt)* has the highest sensitivity to the purely inductive impedance. Therefore, the inductive impedance with 100 kvar is selected for switching in the proposed algorithm.

The main object during determining the impedance value has been selected the lowest amount that can detect the islanding/non-islanding events. Hence, given that the switching impedance is considered as small as possible in this algorithm, the transient changes caused by PII switching strategy are very limited in comparison to other previously introduced active methods as well as other transient events that may frequently occur (such as faults). Therefore, the proposed active method does not have any negative effect on the power quality of the system. It should be noted that if the inductive impedance is selected smaller than 100 kvar, the magnitude of the *FFT(dv/dt)* cannot be large enough to distinguish between islanding and non-islanding conditions.

C. FFT-based Signal Processing Selection

So far various advanced signal processing methods (SPM) have been presented in the literature. The SPM is commonly used to extract hidden features of the passive parameters to reduce NDZ value [26]. Given that, in the proposed scheme, the PII is the principal part of the proposed method which is an active method, without using the common or advanced SPM methods, islanding, and non-islanding events can be detected. Actually, all events can be correctly classified only with tracking the changes in the selected passive parameter. However, this paper uses the *FFT*-based method for more precise analysis of the variations of the selected passive parameter, which is the *FFT(dv/dt)*.

It should be noted that, comparison the magnitude changes of the various frequency components with each other in the wide frequency range shown that the fundamental frequency component has higher sensitivity and accuracy in discriminating between islanding/non-islanding events. Therefore, in simulation studies, the fundamental frequency 60 Hz has been chosen for *FFT* analysis.

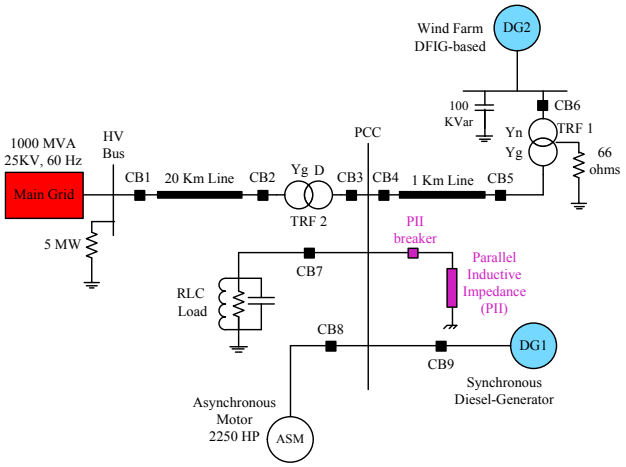

Fig. 3. Schematic diagram of the test system under study.

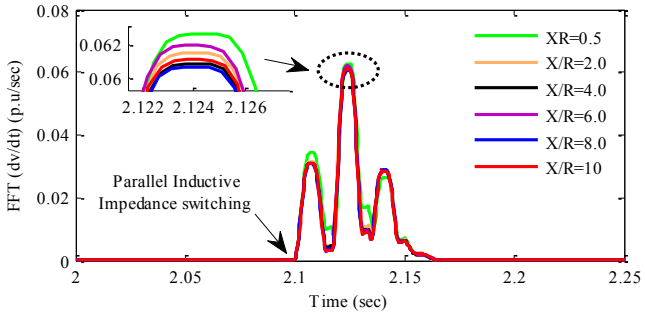

Fig. 4. Simulation results for 100 kvar PII switching in the presence of various X/R ratios.

D. Analytical Investigation of the Proposed Method

To verify the results of the sensitivity analysis carried out in section II-B, the analytical investigation of the proposed method is provided in the following subsection. For this purpose, the impact of the parallel inductive impedance switching on the relationship between the powers and currents at the output of DG, the main grid, and the local load is examined.

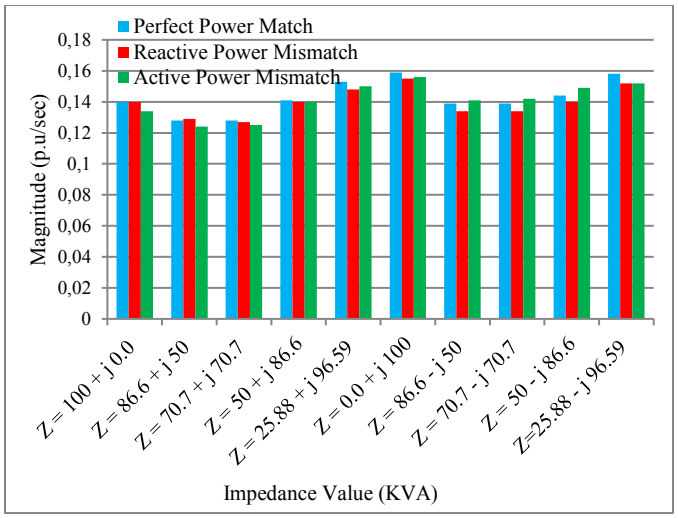

Fig. 5. Maximum changes of the *FFT(dv/dt)* during impedance switching under islanding operating mode.

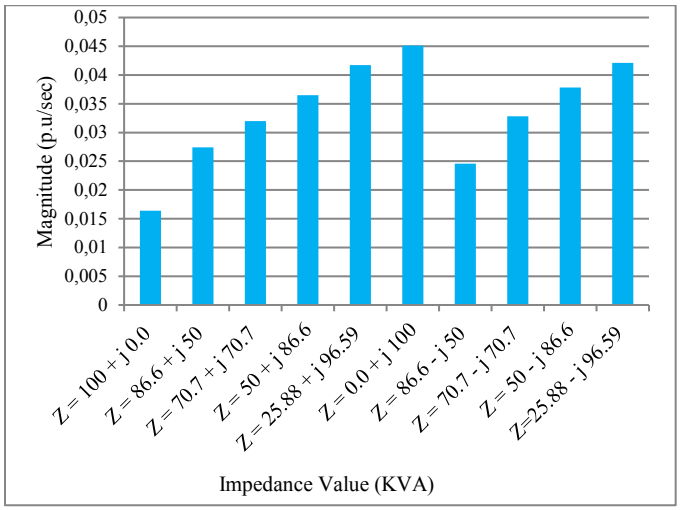

Fig. 6. Maximum changes of the *FFT(dv/dt)* during impedance switching under grid-connected operating mode.

1) Grid-tied operating mode

According to Fig. 1, when DG operates in parallel with the main grid, the relationship between powers and currents at PCC before PII insertion can be defined as follow:

$$\Delta P + j\Delta Q = (P_L - P_{DG}) + j(Q_L - Q_{DG}) \quad (1)$$

$$\Delta I = I_L - I_{DG} \quad (2)$$

Where, ΔP, ΔQ, ΔI, P_L, Q_L, I_L, P_{DG}, Q_{DG}, and I_{DG} denote the difference between the load and DG for active and reactive power and current before PII switching, active and reactive power and current of the load, active and reactive power and current of DG, respectively.

On the other hand, after PII insertion power and currents equations can be defined as:

$$\Delta' P + j\Delta' Q = (P_L - P_{DG}) + j(Q_L + Q_{PII} - Q_{DG}) \quad (3)$$

$$\Delta' I = I_L + I_{PII} - I_{DG} \quad (4)$$

where, $\Delta' P$, $\Delta' Q$, $\Delta' I$, Q_{PII}, and I_{PII} are the difference between the load and DG for active and reactive power, and current after PII switching, reactive power, and current of parallel inductive impedance, respectively.

The relationship between the voltage at PCC (V_{PCC}), DG-side voltage (V_{DG}), and DG-side current (I_{DG}) after PII switching during non-islanding condition is shown in Fig. 7(a). As mentioned earlier, during normal operating mode, the load is supplied by both the DG unit and the main grid. In this situation, according to (3) and (4), by switching the PII, the electrical parameters of the power system are slightly affected. Under this condition, as illustrated in Fig. 7(a), due to the parallel operation of the DG with the main grid, the PCC voltage will be determined by the main grid. As a result, the magnitude of changes of the *FFT(dv/dt)* at V_{PCC} during PII switching at grid-connected mode is very small (as shown in Fig. 2).

2) Islanding mode

According to Fig. 1, after the occurrence of islanding, the relationship between powers and currents at PCC before PII insertion can be defined as:

$$P_{DG} + jQ_{DG} = P_L + jQ_L \quad (5)$$

$$I_{DG} = I_L \quad (6)$$

On the other hand, after the insertion of PII, power and current equations can be expressed as:

$$P'_{DG} + jQ'_{DG} = P_L + j(Q_L + jQ_{PII}) \quad (7)$$

$$I'_{DG} = I_L + I_{PII} \quad (8)$$

Where, P'_{DG}, Q'_{DG}, and I'_{DG} denote the active and reactive power and current of the DG after PII switching, respectively.

The relationship between the V'_{PCC}, V'_{DG}, and I'_{DG} after PII insertion during islanding condition is shown in Fig. 7(b). It is clear that under such circumstances the load is supplied by the DG unit. Thus, the V_{PCC} will be mainly determined by DG. Under this condition, according to (7) and (8), switching the PII will affect the operation of the DG unit. In islanded power systems, due to the limited capacity of the DG plants and their inability in controlling the voltage level as fast as the grid-tied condition, the islanded power systems are more vulnerable to instability rather than grid-tied mode. As a result, inductive impedance switching in islanding conditions can cause large transient changes in PCC voltage.

The above-mentioned modes describe the pattern of the changes of the electrical parameters after applying the

proposed PII strategy. In the following, the changes in V_{PCC} before executing the PII strategy are discussed briefly.

The relationship between active and reactive powers of the load, PCC voltage and load parameters such as R, L, and C are given in (9) and (10) [29].

$$P_L = \frac{V^2 PCC}{R} \tag{9}$$

$$Q_L = V^2 PCC \left(\frac{1}{\omega L} - \omega C\right) \tag{10}$$

According to (9) and (10), the changes in V_{PCC} after the islanding occurrence are affected by P_L and Q_L. Therefore, the small and zero amounts of ΔP and ΔQ cause a slight variation in the V_{PCC}, while the large amount of them causes a significant variation [29]. The previously introduced methods such as [7, 10, 23, 24] proved that regardless the amount of quality factor, the electrical parameters of the power system have a slight change (is not equal to zero) during the islanding with zero power mismatch. In fact, by disconnecting the main grid due to the reconfiguration of the power network a slight transient deviation is occurred in the power system parameters so that the variation magnitude is near to zero but it is not equal to zero.

Therefore, given that the change in V_{PCC} is slight, its rate of change is calculated to better implement the islanding detection condition. By calculating the rate of change of voltage, the insignificant changes in voltage will be more visible to make the decision on the occurred events. However, to improve the clarity of changes during the islanding with perfect power match the frequency analysis is applied to *dv/dt*.

E. Determining the Threshold Values of the FFT(dv/dt)

To determine the threshold values in the proposed method, comprehensive and accurate simulation tests, including islanding and non-islanding events, have been carried out. The results of the tests have illustrated in Fig. 8. The islanding and non-islanding simulated tests are carried out on the test system depicted in Fig. 3. As Fig. 8 reveals, for islanding operating conditions with zero percent power mismatch to 100% power mismatch, the *FFT(dv/dt)* changes are limited to a range between 0.0 p.u/sec to 2.5 p.u/sec. On the other hand, for non-islanding events, the *FFT(dv/dt)* changes are between 0.0 p.u/sec to greater than 2.5 p.u/sec. Therefore, it can be concluded that for *FFT(dv/dt)* greater than 2.5 p.u/sec, the non-islanding condition has occurred. However, since there is an overlap between the value of *FFT(dv/dt)* for both islanding and non-islanding condition in the range of 0.0 p.u/se to 2.5 p.u/se, to distinguish between the islanding and non-islanding conditions, the PII switching will be activated. For this purpose, to determine the value of *FFT(dv/dt)* after PII switching, a set of simulations have been carried out and their results are recorded, while the PII is switched on and off for both islanding and non-islanding conditions. As illustrated in Fig. 8, after the activation of the PII, the value of the *FFT(dv/dt)* for all non-islanding conditions is much smaller than 0.1 p.u/sec, whereas the *FFT(dv/dt)*changes for islanding condition is greater than 0.1 p.u/sec. Therefore, in the proposed scheme, the threshold value for Set_{BIS} is set to 2.5 p.u/sec, and Set_{AIS} is set to 0.1 pu/sec.

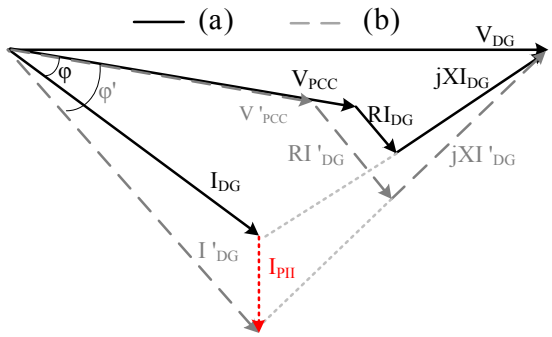

Fig. 7. The relationship between the voltages and currents signals during PII switching, (a): grid-tied operating mode, (b): islanding operating mode.

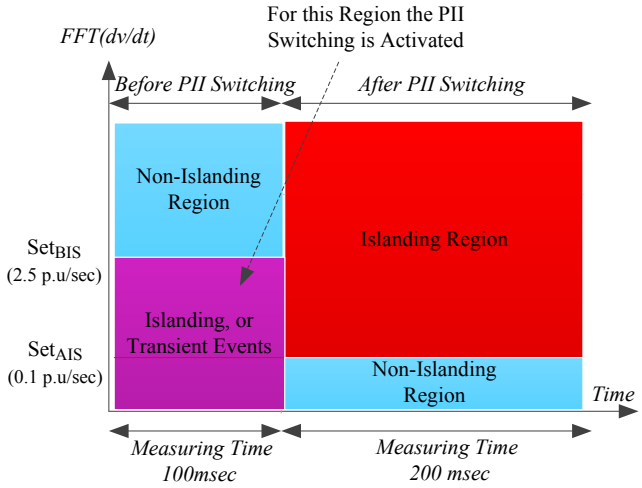

Fig. 8. Detection regions of the proposed scheme for various *FFT(dv/dt)*.

F. Flowchart of the Proposed Method

Flowchart of the proposed method is presented in Fig. 9. At first, the voltage at PCC is measured, and its rate of change is calculated. Whenever any changes observed in the *FFT(dv/dt)*, the magnitude of these changes is measured for 100 *msec*. If the change in $FFT(dv/dt)_{BIS}$ parameter exceeds the Set_{BIS} value, the proposed method identifies this condition as a non-islanding condition. On the other hand, if the magnitude of the $FFT(dv/dt)_{BIS}$ changes are smaller than Set_{BIS}, the change in the $FFT(dv/dt)_{BIS}$ can be considered as the result of an islanding or other transient conditions. To address this issue, the parallel inductive impedance is switched on and then immediately switched off. Then, the magnitude of the *FFT(dv/dt)* changes are measured for 200 *msec*. If the magnitude of the $FFT(dv/dt)_{AIS}$, exceeds the Set_{AIS} value, the islanding condition is detected. Otherwise, the non-islanding event occurs.

It should be noted that in the proposed method the $FFT(dv/dt)_{BIS}$ and $FFT(dv/dt)_{AIS}$ are maximum magnitude changes of *FFT(dv/dt)* before and after impedance switching, respectively.

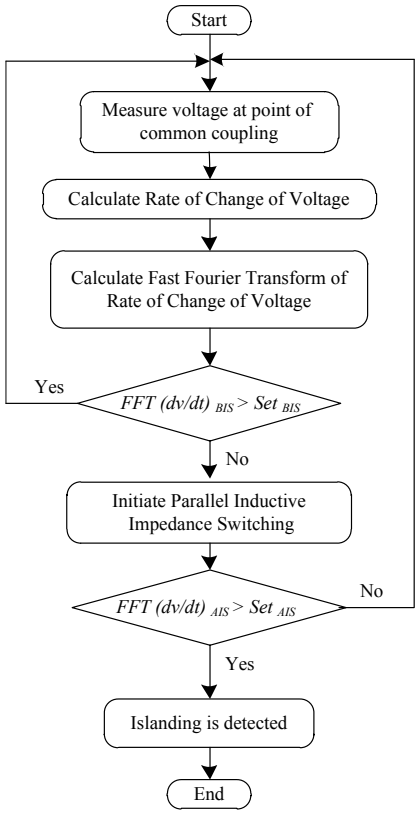

Fig. 9. Flowchart of the proposed islanding detection scheme.

III. Results and Discussion

The single line diagram of the test system is shown in Fig. 3 and all the simulation parameters are presented in Table I. As shown in Fig. 3, the DG1 is the synchronous type and is connected to the PCC through CB9. Also, the DG2 is inverter-based and is connected to the PCC through a step-up transformer and small distribution line. To demonstrate the effectiveness of the proposed method, a comprehensive simulation study based on the available standards is carried out under different operating conditions.

TABLE I
Simulation Parameters

Grid		*1000 MVA, f = 60 Hz, V_n = 25 kV* *X/R = 10*
DG	*DG2*	*1.5 MW, 575 V, 60 Hz*
	DG1	*3.125 MVA, 60 Hz, 2400 V* *Woodward governor model* *IEEE AC1A-type exciter*
Transformers	*TR1*	*4 MVA, 575/2400 V* *$R_1 = R_2 = 0.025/30$ p.u* *$L_1 = L_2 = 0.025$ p.u ,* *$R_m = X_m = 500$ p.u.*
	TR2	*6MVA, 25/2.4 KV* *R1 = R2 = 0.0015 p.u* *$L_1 = L_2 = 0.03$ p.u* *$R_m = X_m = 200$ p.u*
Distribution Line		*$R_1 = 0.1153$ Ω/Km, $R_0 = 0.413$ Ω/Km* *$L_1 = 1.05\times10^{-3}$ H/Km, $L_0 = 3.32\times10^{-3}$ H/Km* *$C_1 = 11.33\times10^{-9}$ F/Km, $C_0 = 5.01\times10^{-9}$ F/Km*
Induction Motor		*2250 HP, V_n = 2400 v* *$R_s = 0.029$ p.u, $R_r = 0.022$ p.u* *$L_r = L_s = 0.266/377$ p.u, $L_m = 13.04/377$ p.u*
Load Default Parameters		*R =2.304 (Ω), L=0.00313 (H),* *C=1895.6 (μf), Q_f=1.8*

The corresponding results are provided in the following subsections. It should be noted that in all the simulation cases, islanding and non-islanding events occur at the 2 sec.

A. Scenario 1: Islanding Occurrence

The efficiency of islanding detection methods can be seriously impaired by the perfect power match or minor power mismatch conditions as well as the quality factor of loads. Therefore, to conduct an in-depth investigation of the proposed method, two sets of tests have been done. The first one group include zero, minor and major power mismatches of active and reactive power with constant quality factor Q_f= 1.8. The second one group tests include perfect and minor power mismatches with various quality factors. It should be noted that the reasonable value of quality factor that has been presented by IEEE 1547.1 standard and previous researches usually is smaller than or equal to 2.5 [28, 29]. Hence, in this part, the Q_f is considered in the range between 0.5 to 2.5. The corresponding results are present in either case of power mismatch (zero, minor or major), the value of the $FFT(dv/dt)_{BIS}$ is smaller than Set_{BIS}. Therefore, the proposed algorithm detects the situation as an abnormal condition and proceed to explore the power system status. Accordingly, in all considered circumstances, PII switching is triggered. The obtained results in Tables II and III indicate that in all conditions following the PII switching, the value of the $FFT(dv/dt)_{AIS}$ is greater than Set_{AIS}. As a result, the proposed islanding detection scheme is capable of identifying all circumstances of islanding effectively, even under perfect power match condition with various Q_f. As mentioned in part II. B, the proposed active PII strategy performance is not affected by various Quality factors. Thus, the non-detection zone is completely eliminated from the proposed scheme.

TABLE II
Simulation Results for Islanding Occurrence Considering Different Power Mismatches with Various Quality Factors

Mismatch value	Qf	load value (Ω, H, μf)	$FFT(dv/dt)_{BIS}$	$FFT(dv/dt)_{AIS}$
0.0 MW + j 0.0 MVAr (Perfect Active and Reactive Powers Match)	0.5	R=11.520 L=0.0611 C=92.150	0.404	0.151
	1.2	R=5.7610 L=0.0127 C=184.30	0.148	0.145
	2.0	R=3.8410 L=0.0019 C=442.47	0.037	0.135
	2.5	R=2.8810 L=0.0021 C=923.45	0.032	0.155
0.2 MW + j 0.2 MVAr (Active and Reactive powers mismatch)	0.5	R=2.3040 L=0.0122 C=435.02	0.496	0.154
	1.2	R=2.3040 L=0.0253 C=975.62	0.281	0.152
	2.0	R=2.3040 L=0.0030 C=1782.1	0.178	0.153
	2.5	R=2.3040 L=0.0024 C=2086.1	0.127	0.152

To illustrate the dynamic variation of the *FFT(dv/dt)* signal during islanding occurrence, some of the test results provided in Tables II and III graphically depicted in Figs. 10 and 11, respectively.

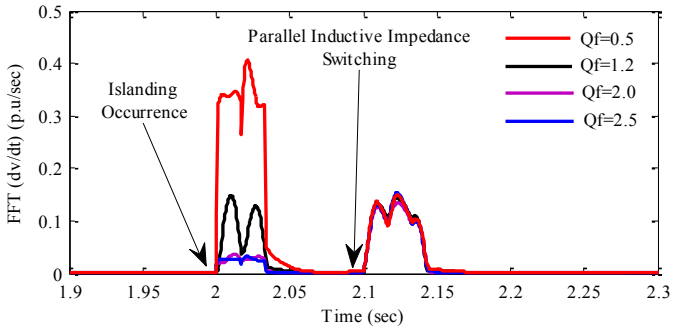

Fig. 10. Simulation results for islanding with perfect power match with various quality factors.

TABLE III
Simulation Results for Islanding Occurrence with Different Power Mismatches and Constant Quality Factor

Test Type	Test No	Mismatch (MVA)	*FFT(dv/dt)* $_{BIS}$	*FFT(dv/dt)* $_{AIS}$
Active and reactive Power Mismatch	1	0.0 + j 0.0	0.051	0.157
	2	0.1 + j 0.1	0.052	0.155
	3	0.2 + j 0.2	0.133	0.153
	4	0.3 + j 0.3	0.220	0.150
	5	0.4 + j 0.4	0.305	0.151
	6	1.0 + j 1.0	0.782	0.140
	7	2.0 + j 2.0	1.475	0.134
	8	3.0 + j 3.0	2.085	0.127
Reactive Power Mismatch	21	0.0 + j 0.1	0.035	0.157
	22	0.0 + j 0.2	0.042	0.152
	23	0.0 + j 0.3	0.067	0.154
	24	0.0 + j 0.4	0.093	0.153
	25	0.0 + j 1.0	0.254	0.144
	26	0.0 + j 2.0	0.490	0.137
	27	0.0 + j 3.0	0.695	0.134
Active Power Mismatch	28	0.1 + j 0.0	0.064	0.156
	29	0.2 + j 0.0	0.122	0.156
	30	0.3 + j 0.0	0.194	0.155
	31	0.4 + j 0.0	0.271	0.155
	32	1.0 + j 0.0	0.714	0.148
	33	2.0 + j 0.0	1.414	0.146
	34	3.0 + j 0.0	2.073	0.148

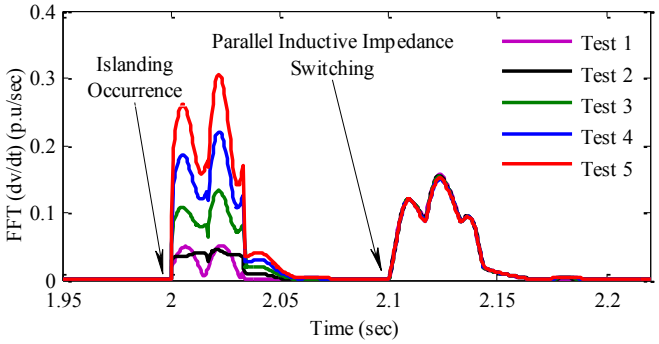

Fig. 11. Simulation results for islanding with various power mismatches and constant quality factor.

B. Scenario 2: Capacitor Switching

The instant in which either the capacitor is switched on or off, the electrical parameters of the power system change, which could jeopardize the proper operation of the proposed approach. In this section, the performance of the proposed method has been investigated against capacitor switching for different capacities. The obtained results are presented in Table IV. As can be seen, for small capacitor values, the $FFT(dv/dt)_{BIS}$ is small, and for a large capacity value, it is substantial. However, for all capacitor switching tests, the value of the $FFT(dv/dt)_{BIS}$ is smaller than Set_{BIS}. By means of the PII switching, it is observed that in all circumstances in which capacitor is connected or disconnected, the magnitude of the $FFT(dv/dt)_{AIS}$ is smaller than Set_{AIS}. Thus, the proposed method is capable of identifying all these conditions as a non-islanding event. Likewise, the dynamic variation of the *FFT(dv/dt)* for some of the results is plotted in Fig. 12.

TABLE IV
Simulation Results for Capacitor Switching with Different Capacities

Test Type	Test No	Capacitor Capacity	*FFT(dv/dt)* $_{BIS}$	*FFT(dv/dt)* $_{AIS}$
Switch ON	1	0.4 MVAr	0.138	0.044
	2	0.8 MVAr	0.277	0.045
	3	1.2 MVAr	0.416	0.044
	4	1.6 MVAr	0.577	0.045
	5	2.0 MVAr	0.699	0.044
	6	3.0 MVAr	1.055	0.044
	7	4.0 MVAr	1.416	0.044
Switch OFF	9	0.4 MVAr	0.138	0.044
	10	0.8 MVAr	0.277	0.044
	11	1.2 MVAr	0.416	0.043
	12	1.6 MVAr	0.555	0.045
	13	2.0 MVAr	0.696	0.044
	14	3.0 MVAr	1.055	0.045
	15	4.0 MVAr	1.417	0.047

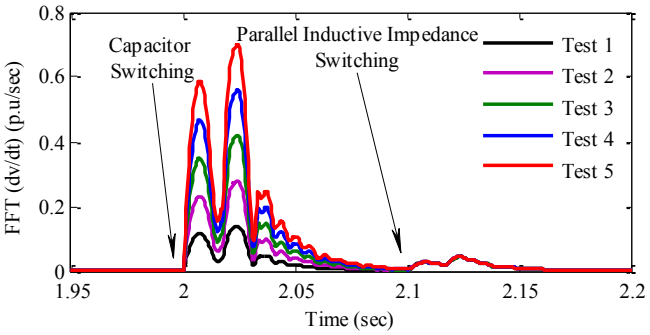

Fig. 12. Simulation results for capacitor switching with various capacities.

C. Scenario 3: Short Circuit Fault Occurrence

The short circuit fault occurrence may mislead the performance of the proposed method to the false detection of islanding condition. In this section, the performance of the proposed method has been assessed for various short circuit faults, i.e., open conductor fault, single-, double-, and three-phase faults with different fault impedance values ranging from 0 to 20 Ω which lasts for four cycles. It should be noted that open-conductor fault tests are applied to the 20Km line in Fig. 3. The obtained results are presented in Tables V and VI.

C.1. Single-, double-, and three-phase faults: As can be seen from Table V, for R_f between zero and 8 Ω in single-phase fault, and for R_f = 0 and 2 Ω in double-phase fault, and for R_f = 0 Ω in three-phase fault, the $FFT(dv/dt)_{BIS}$ exceeds Set_{BIS} which can be classified as non-islanding events according to the proposed method. On the other hand, for all other tests, the value of the $FFT(dv/dt)_{BIS}$ is smaller than Set_{BIS}.

Therefore, by switching PII, it can be seen that in all circumstances the maximum value of the $FFT(dv/dt)_{AIS}$ is smaller than Set_{AIS}, which indicates that all conditions are correctly identified as a non-islanding event. The dynamic variation of the *FFT(dv/dt)* for three-phase to ground faults (LLLG) of the tests results in Table V is plotted in Fig. 13.

C.2. Open-conductor faults: Since the open conductor faults act as a high impedance fault, changes in the electrical parameters such as voltage and current are slight. As reported in Table VI, to investigate the proposed method performance, three types of open conductor fault (one-conductor, two-conductor, and three-conductor) at different distances from the line to PCC bus include first-line (1Km), mid-line (10 Km), and end-line (19 Km) are considered. As it can be seen from the results, changes in the $FFT(dv/dt)_{BIS}$ in all states lie very smaller than the Set_{BIS}. Therefore, by applying the PII strategy, *the* maximum value of the $FFT(dv/dt)_{AIS}$ is smaller than Set_{AIS} in all tests. Thus, all types of open-conductor faults can precisely be classified as non-islanding events by the proposed method. It should be noted that the location of the open-conductor fault does not have any negative effect on the proposed islanding detection method performance, because based on the data reported in Table VI, changes in the *FFT(dv/dt)* for a different location at similar open-conductor faults are very close together.

TABLE V
Simulation Results For Short-Circuit Faults with Different Resistances Value

Fault Type	Test No	R_f	$FFT(dv/dt)_{BIS}$	$FFT(dv/dt)_{AIS}$
Single-phase fault	1	0.0 Ω	33.15	-
	2	2.0 Ω	7.728	-
	3	4.0 Ω	5.038	-
	4	6.0 Ω	3.731	-
	5	8.0 Ω	2.961	-
	6	10 Ω	2.451	0.046
	7	12 Ω	2.094	0.046
	8	14 Ω	1.828	0.045
	9	16 Ω	1.619	0.044
	10	18 Ω	1.455	0.044
	11	20 Ω	1.321	0.043
Double-phase fault	12	0.0 Ω	42.05	-
	13	2.0 Ω	3.234	-
	14	4.0 Ω	2.445	0.045
	15	6.0 Ω	1.974	0.045
	16	8.0 Ω	1.657	0.044
	17	10 Ω	1.427	0.044
	18	12 Ω	1.253	0.045
	19	14 Ω	1.119	0.043
	20	16 Ω	1.009	0.045
	21	18 Ω	0.918	0.044
	22	20 Ω	0.842	0.044
Three-phase fault	23	0.0 Ω	39.6	-
	24	2.0 Ω	0.470	0.042
	25	4.0 Ω	0.236	0.043
	26	6.0 Ω	0.157	0.043
	27	8.0 Ω	0.118	0.043
	28	10 Ω	0.094	0.043
	29	12 Ω	0.078	0.044
	30	14 Ω	0.067	0.043
	31	16 Ω	0.059	0.044
	32	18 Ω	0.052	0.044
	33	20 Ω	0.047	0.043

The dynamic variation of the *FFT(dv/dt)* for open-conductor faults in Table VI is plotted in Fig. 14.

TABLE VI
Simulation Results for Open-Conductor Faults at Different Locations with the Various States of Open-Conductors.

Test Type	Test No	Fault Location	$FFT(dv/dt)_{BIS}$	$FFT(dv/dt)_{AIS}$
One-Conductor Open	1	First-line	0.009	0.045
	2	Mid-line	0.008	0.044
	3	End-line	0.007	0.044
Two-Conductor Open	4	First-line	0.019	0.044
	5	Mid-line	0.017	0.044
	6	End-line	0.015	0.043
Three-Conductor Open	7	First-line	0.019	0.044
	8	Mid-line	0.018	0.044
	9	End-line	0.018	0.044

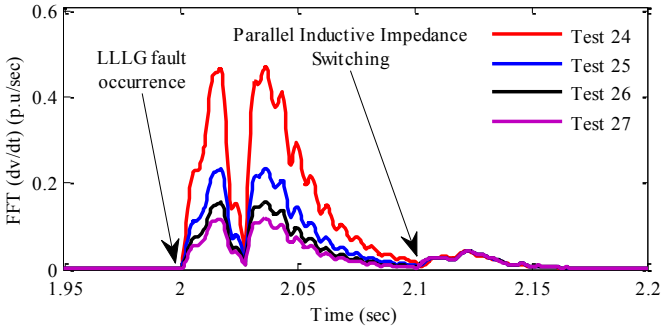

Fig. 13. Simulation results for three-phase fault with various fault impedances.

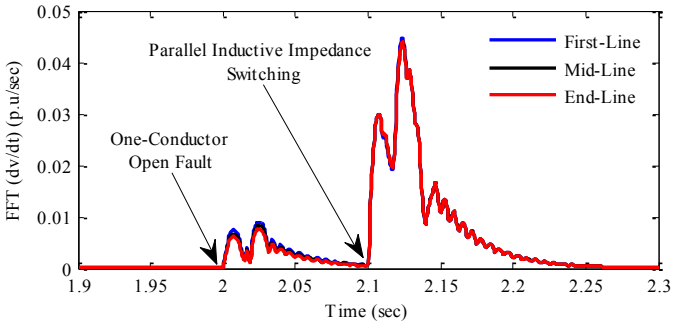

Fig. 14. Simulation results for the one-conductor open fault at different locations.

D. Scenario 4: Motor Switching

The instant in which the motor is switched either on or off, the electrical parameters of the power system change. These changes may result in interference with DGs islanding detection. Therefore, in this section, the performance of the proposed method has been investigated during induction motor switching for different power levels. The obtained results are summarised in Table VII. As it can be seen from Table VII, in all tests of induction motor starting, the value of the $FFT(dv/dt)_{BIS}$ exceeds Set_{BIS}. Therefore, it is not required to activate PII switching, and only by making use of *FFT(dv/dt),* the non-islanding condition is detected. In all cases of the motor being switched out, $FFT(dv/dt)_{BIS}$ is smaller than $Set_{BIS,}$ which indicates that PII switching is activated. It can be seen in all cases, $FFT(dv/dt)_{AIS}$ is lower than Set_{AIS}, and conditions are detected accurately. In fact, the proposed method correctly identifies all cases as non-islanding events. The dynamic

variation of the *FFT(dv/dt)* for some of the tests results in Table VII is plotted in Fig. 15.

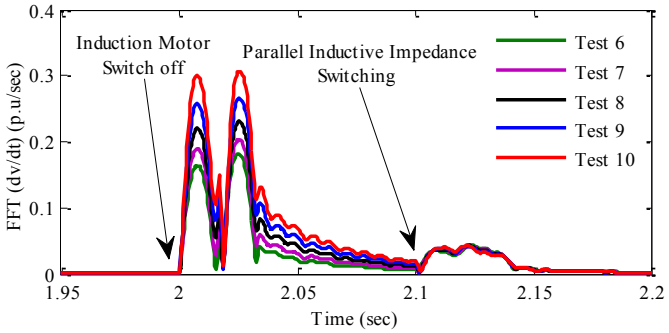

Fig. 15. Simulation results for induction motor switching with various powers.

TABLE VII
Simulation Results for Induction Motor Switching with Different Power Levels

Test Type	Test No	Power Level	$FFT(dv/dt)_{BIS}$	$FFT(dv/dt)_{AIS}$
Switch ON	1	400 HP	4.464	-
	2	800 HP	4.990	-
	3	1200 HP	6.730	-
	4	1600 HP	6.578	-
	5	2000 HP	5.695	-
Switch OFF	6	400 HP	0.182	0.044
	7	800 HP	0.203	0.042
	8	1200 HP	0.231	0.041
	9	1600 HP	0.264	0.042
	10	2000 HP	0.306	0.042

E. Scenario 5: Load Changing

The regular load changing can cause transient variations in the electrical parameters and may lead to the failure of islanding detection. In this section, the effects of various loads changing at different power levels, power factor and quality factor on the performance of the proposed method are evaluated. The obtained results are presented in Table VIII. As it can be seen from Table VIII, in all cases that the load changes, the $FFT(dv/dt)_{BIS}$ is smaller than Set_{BIS}. Hence, the PII switching is activated. Accordingly, as shown in Table VIII, the value of the $FFT(dv/dt)_{AIS}$ is smaller than Set_{AIS}. As a result, the proposed scheme correctly identifies all cases as a non-islanding event. Therefore, the operation of the proposed method is not affected by load changing with various powers, power factor and quality factor. For more clarity, some of the results during load-changing scenario are presented in Fig. 16.

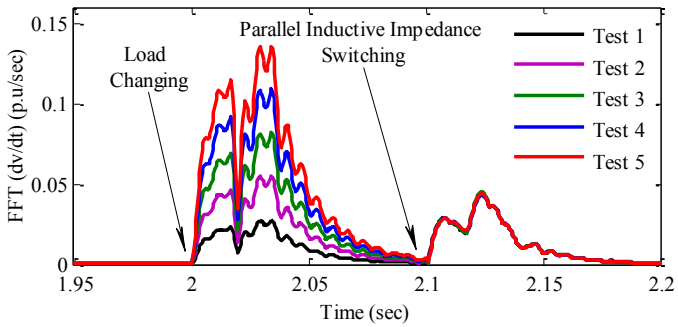

Fig. 16. Simulation results for load changing with various powers.

TABLE VIII
Simulation Results for Load Changing with Different Levels of Active and Reactive Powers

Test No	Power Level	$FFT(dv/dt)_{BIS}$	$FFT(dv/dt)_{AIS}$
1	0.2 MW	0.027	0.044
2	0.4 MW	0.054	0.043
3	0.6 MW	0.081	0.045
4	0.8 MW	0.109	0.043
5	1.0 MW	0.135	0.043
6	0.5 + j 0.5 MVA	0.211	0.043
7	1.0 + j 1.0 MVA	0.420	0.043
8	1.5 + j 1.5 MVA	0.627	0.042
9	2.0 + j 2.0 MVA	0.831	0.041
10	2.5 + j 2.5 MVA	1.033	0.041

IV. Comparison Of The Proposed Method And Other Existing Approaches

The proposed method has been assessed on a power system in the presence of synchronous- and inverter-based DG units during various scenarios of islanding and non-islanding events. The results show that the proposed method can easily detect all islanding and non-islanding conditions for any type of DGs, such as inverter-based and synchronous-based. Some merits of this method in comparison with other existing methods can be summarized as follow:

- First and foremost, as illustrated in the simulation section, the non-detection zone of the proposed method is completely eliminated, while the proposed methods in [3], [4], [9], and [21] have a significant NDZ value. So, the proposed scheme can be considered as an accurate and efficient method in comparison with previously introduced ones.
- One of the other most important indexes for islanding detection methods assessment is the detection time. As presented in part II.F and proved by simulation studies in part III, the total time required for both passive and active part of the suggested method to discriminate between islanding and other transient events is 300 msec (100 msec for passive part and 200 msec for active part) for the worst case scenario that active part is activated. It should be noted that, as it can be seen from the simulation data, some conditions can be identified only by the passive part which has required 100 msec for detection. While, the detection time of the suggested methods in [3], [4], [20], [21], and [27] are around 900 msec, 500 msec, 420 msec, 480 msec, and 425 msec, respectively.
- Unlike the introduced method in [24] that uses the breaker switching at DG output, the proposed scheme implements the breaker switching at inserted PII connection point. In practical conditions, generally, the recloser at the DG output is set to off mode due to some technical problems it can raise, such as short circuit level, instability of DG unit. Therefore, the PII is practically viable and does not have any adverse effect on the stability of the power system.
- Unlike the methods that are applicable to certain types of DG units, the proposed scheme in this paper can be employed for any kind of DGs. For instance, the methods in [14], [24] is only valid for the synchronous DGs, and the procedures outlined in [15], [16] are just applicable to the inverter-based DGs.

- Unlike to previous methods that cause a disturbance in the power system, like those introduced in [17], and [21] the suggested technique in this paper does not have any adverse effect on the operation of the power system such as reducing power quality and causing disturbance due to very small impedance switching.

V. CONCLUSION

This paper presents a novel islanding detection scheme based on *FFT* applied to the rate of change of voltage and parallel inductive impedance switching. By means of the inductive impedance switching, the *FFT(dv/dt)* variations can be used to distinguish between islanding and non-islanding events. To demonstrate the efficiency of the proposed scheme, an analytical investigation of the proposed scheme is provided. Moreover, a set of the simulations is carried out under different operational conditions whose obtained results indicate that even under the worst circumstances of events conditions, the proposed scheme is able to easily and effectively distinguish between the islanding and other power system disturbances.

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