Rautiainen, Antti; Vuorinen, Vesa; Heikkinen, Hannele; Paulasto-Krockel, Mervi

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Wafer-Level AuSn/Pt Solid–Liquid Interdiffusion Bonding

Antti Rautiainen, Vesa Vuorinen, Hannele Heikkinen, and Mervi Paulasto-Kröckel, Member, IEEE

Abstract—In this paper, wafer-level AuSn/Pt solid–liquid interdiffusion bonding for hermetic encapsulation of microelectromechanical systems (MEMS) is evaluated. Although AuSn is used for bonding of ICs, the implementation of AuSn diffusion bonding in MEMS applications requires thorough understanding of its compatibility with the complete layer stack including adhesion, buffer, and metallization layers. Partitioning of the layer stacks is possible in MEMS devices consisting of several silicon wafers since the device wafer carrying functional structures and the encapsulation wafer have different restrictions on process integration and applicable metal deposition techniques. In this paper, CMOS/MEMS compatible sputtered platinum is utilized on the device wafer as a contact metallization for Au–Sn metallized cap wafer. The role of the platinum layer thickness as well as the nickel and molybdenum buffer layers on mechanical reliability were tested. The mechanical shear and tensile tests were performed for samples after bonding as well as after high-temperature storage and thermal shock tests. The results were rationalized based on the combined microstructural, thermodynamic, and fracture surface analyses. High-strength and thermodynamically stable bonds were achieved, exhibiting shear strength up to \( \sim 180 \text{ MPa} \) and tensile strength up to \( \sim 80 \text{ MPa} \). Platinum was consumed completely during bonding and was observed to dissolve mainly into the \((\text{Au,Pt})\text{Sn}\) phase. Thicker platinum layer (200 versus 100 nm) increased the \((\text{Au,Pt})\text{Sn}\) phase thickness and resulted in higher strength. The molybdenum buffer layer under the platinum metallization increased the tensile strength significantly.

Index Terms—Au–Sn–Pt system, intermetallic compounds (IMCs), remelting temperature, solid–liquid interdiffusion (SLID) bonding.

I. INTRODUCTION

Wafer bonding is a key process for 3-D integration that will sustain the performance progress of electronics by the “More-than-Moore” approach [1], [2]. Smart sensors for this platform are founded on microelectromechanical systems (MEMS) that operate under vacuum or controlled atmosphere conditions, and efficient wafer-level hermetic MEMS packaging requires similar processes, yield, and reliability as the 3-D integration overall [2], [3]. Traditional wafer bonding techniques, such as direct, anodic, and glass-frit bonding, are challenging for wafer-level vacuum packaging of the smart sensors when CMOS wafer needs to be integrated into the system [3], [4]. Meanwhile, metal interconnections offer a solution to bond several types of wafers within CMOS thermal budget. In addition, the possibility to combine hermetic sealing and electrical interconnections for through-silicon vias within the same process flow is a major benefit [3]–[5].

Solid–liquid interdiffusion (SLID) bonding utilizes a fluxless bonding protocol resulting in a high remelting temperature, and it possesses excellent hermeticity along with a high tolerance for metal surface conditions and results in high-strength bonds [3], [4], [6], [7]. In SLID bonding, which is also known as transient liquid phase bonding [4], [8], [9], a low-melting-point metal (e.g., Sn) is reacting with a high-melting point metal (e.g., Au, Pt, and Cu) until all the former is consumed to intermetallic compounds (IMCs) that have elevated melting temperatures. However, depositing several-micrometers-thick layers of the typically used high-melting-point metals (Au and Cu) is challenging on MEMS device or CMOS/ASIC wafers from the process integration point of view. In addition, thick gold metallizations are required, if elevated remelting temperature is desired with Au–Sn SLID bonding, which increases the cost significantly. Therefore, platinum, often used in various optoelectronic and power electronic applications applying Au–Sn fluxless soldering [10]–[20], was selected as a noble device wafer contact metallization in this paper.

Platinum has been studied as a barrier metal for eutectic Au–Sn solder, nonetheless the experimental results indicate a rapid dissolution of the Pt into the Au–Sn system [19]–[24], which raises the remelting temperature of the solder [21], [24], [25]. The increase of the remelting temperature is one of the main advantages of the SLID bonding, as it enables further high-temperature processing, such as subsequent assembly steps and getter activation (> 300 °C ∼ 15 min) of MEMS devices [4], and it also enhances the reliability at high operational temperatures. The rapid dissolution also reduces the required bonding time. Even a small amount of dissolved platinum into the eutectic AuSn solder elevates the remelting temperature based on the existing experimental and thermodynamic data [21], [25].

In this paper, platinum-based metallizations on the MEMS device wafer are designed from manufacturability, reliability,
and cost viewpoints for SLID bonding with a gold–tin metallized cap wafer based on the thermodynamic data [25]. Molybdenum can be utilized as a redistribution layer or a buffer layer under the platinum contact metallization. Molybdenum is also a superb material for hermetic devices due to its thermal stability, high density, and low vapor pressure supporting the excellent performance in MEMS applications for harsh environments. Thus, molybdenum has been utilized in MEMS applications [26], [27]. The influence of both Pt-layer thicknesses and the presence of Mo layer are evaluated in this paper. The effect of cap wafer (aka encapsulation/top wafer) nickel barrier layer on mechanical strength is assessed as well, as it has been shown to increase the mechanical strength of the symmetrical Au–Sn/ Sn–Au SLID bonds [6], and also enhance the electrical and mechanical performance in Au–Sn soldering [12], [16], [21]. Nickel was not used as a contact metallization on MEMS wafer, as it forms stable oxide/hydroxide, which worsens wetting and has an impact on shelf life. In order to resolve this issue, it would require significant cleaning steps that would not be suitable for processed MEMS wafers. The interfacial compatibility and mechanical reliability of the bonds are investigated with shear and tensile tests carried out on both as-bonded and aged samples. The results are rationalized based on the combined microstructural, thermodynamic, and fracture surface analyses.

II. MATERIALS AND METHODS

Standard double-side-polished 150-mm silicon wafers (thickness 400 µm) were used as cap wafers, and 150-mm single-side-polished wafers (thickness 675 µm) were used as device wafers. Both wafer types were (100) with p-doping and thermally oxidized, and were manufactured by Okmetic Oyj. The bonding schemes and the used abbreviations for the four sample groups are presented in Fig. 1. A 40-nm TiW (10/90 wt-%) layer was sputtered as an adhesion layer between the silicon and a 100-nm-thick gold seed layer on cap wafers. Prior to the seed layer deposition in groups B–D, a 200-nm-thick nickel film was sputtered on cap wafers. A 4-µm-thick gold was electroplated to the resist openings, and a 2-µm-thick tin layer was electroplated on the top of the Au layer on the cap wafers. The seal ring geometry was a round-edge rectangle with dimensions of 1650 µm (aka “long side”) × 625 µm (aka “short side”), and the width of the ring was 80 µm. More details for the cap wafer manufacturing can be found from [6], [28], and [29].

In groups A and B, a 100-nm-thick sputtered Pt layer was used on the device wafer, and in groups C and D, this layer thickness was increased to 200 nm. Titanium adhesion layer (40 nm) was sputtered prior to the platinum, and within the groups A, B, and D, 40-nm titanium/200-nm molybdenum metallization layers were deposited prior to the Ti/Pt layers. Device wafer metallizations (Ti and Pt) were patterned with a lift-off process, and prior to the bonding, seed metallization on the cap wafer was etched. Wafers were aligned and assembled on a bonding chuck with an EVG620 bond aligner and bonded with an EVG501 wafer bonder for 30 min at 320 °C with 3.3-MPa bonding pressure. Wafers were diced into 5 mm × 5 mm chips after the bonding process.

For the cross-sectional analysis, the samples were prepared using standard metallographic methods. The analysis was performed with a JEOL JSM-6330F field emission scanning electron microscope (SEM) with Oxford Instruments INCA X-sight energy-dispersive X-ray spectroscopy (EDS) equipment. The EDS analysis was performed from a minimum of five locations for each phase. Fracture surface analysis was performed based on the area analysis of fracture surfaces with the same SEM. Scanning transmission electron microscopy (STEM) utilizing a high-angle annular dark-field detector and an EDX (EDAX) was performed at 200 kV with an FEI Tecnai F20-FEGTEM S-Twin microscope, and the electron-transparent lamella was prepared by a focused ion beam (FIB) system (TESCAN LYRA3).

The shear test was carried out with an MTS 858 Table System that contained a Flex Test 40 Digital controller and an MTS SilentFlow HPU system. The detailed experimental setup is presented in [6]. The test was shear strain controlled with 0.01-mm/s rate. A stud pull method was used to characterize the tensile strength of the bonds with the same MTS system. The test setup is presented in detail in [6], and the test was performed with a strain rate of 0.1 mm/s. A minimum of five samples were tested per condition. In tensile test, the samples failing within the fixing glue were excluded from the analysis.

The high-temperature storage (HTS) aging test was conducted with a Heraeus Instruments oven for 1000 h at 150 °C. The thermal shock (TS) test was performed with an ESPEC TSA-71 S TS chamber system. The operational temperature range was −40 °C to +125 °C with 33 °C/min ramp rate, 10-min dwell time, for both high and low temperatures, and a total cycle time of 30 min. Samples were exposed to 1000 cycles. TS test was performed according to JEDEC JESD22-A104D standard with test condition G and soak mode 3.

III. RESULTS

A. Microstructural Analysis

Micrographs of as-bonded samples are presented in Fig. 2(a)–(d). The bond microstructure was majorly the
same in all groups consisting of Au₅Sn (Au₈₆Sn₁₄ at-%) and (Au,Pt)Sn (Au₃₀Pt₁₉Sn₅₁ at-%) phases. The observed average Pt solubility of 19 at-% in the (Au,Pt)Sn phase is well in line with the recent thermodynamic reassessment of the Au–Pt–Sn system [25]. In addition, a solubility of ∼2 at-% Pt was detected in the Au₅Sn phase that is in local equilibrium with the (Au,Pt)Sn phase, as shown in Fig. 2(e). Within groups A and B, the (Au,Pt)Sn phase was not uniform and the Au₅Sn phase was detected to reach the device wafer Ti/Mo metallization. However, with thicker platinum metallization in groups C and D, the (Au,Pt)Sn phase was observed to be thicker and more uniform. The 200-nm nickel barrier between the TiW and the seed Au layer (groups B–D) on the cap wafer side was completely consumed during bonding, and formed the (Ni,Au)₃Sn₂ phase (Ni₃₅Au₁₉Sn₄₆ at-%, [30]) at the interface, as also observed with the Au–Sn SLID bonds [6]. Thickness of this layer was similar between groups B and D. Molybdenum did not react with the IMCs, as it can be observed as a uniform layer between the bond and SiO₂ within groups A, B, and D samples (see Fig. 2).

As can be seen in Fig. 2(e), there is clearly an additional phase with a bright contrast between the (Au,Pt)Sn phase and Ti/Mo metallization. STEM with EDX was utilized for investigating this phase more in detail. Micrographs of STEM analysis are presented in Fig. 3(a)–(d). The fit elemental analysis linescan is presented in Fig. 3(e), and results indicated that the bright phase is an Au₄Ti phase with a small solubility of Sn between the (Au,Pt)Sn and Ti/Mo during the bonding process.

There were no observable changes in the microstructures of the bonds under the HTS test. During annealing, the layer thicknesses remained practically the same; no new phases were observed, and there were not any significant changes in the solubility of the third element in the (Au, Pt)Sn, Au₅Sn, and (Ni, Au)₃Sn₂ phases. In addition, molybdenum acts as a barrier against Au–Sn/Pt bond and Ti/SiO₂ as it can be found as an initial ∼200-nm-thick layer within the samples also after 1000-h annealing at 150 °C, as also observed in [33]. Neither the TiW nor molybdenum reacted with the IMCs at 150 °C, thus the bonds are thermodynamically stable after the bonding process. However, after the TS test within a few group C samples, cracks were observed at two locations: between the TiW and (Ni,Au)₃Sn₂ layers on cap wafer side and at the device wafer interface (between the Au₄Ti[Sn] layer and Ti/SiO₂). These observations are presented in Fig. 4. In other groups, cracks were not detected.

**B. Thermodynamic Analysis**

There were no significant changes in the bond microstructures during annealing at 150 °C for 1000 h, highlighting the thermal stability of the SLID bonds. The IMC
Fig. 4. Cracks observed within a few group C samples after the TS test. (a) Crack between TiW layer and the (Ni,Au)\textsubscript{3}Sn\textsubscript{2} phase. (b) Crack between the Au\textsubscript{4}Ti\textsubscript{Sn} phase and Ti/SiO\textsubscript{2}. (c) High-magnification image of the device wafer interface showing a crack.

Reactions occurred already during the bonding process by forming Au\textsubscript{3}Sn and (Au,Pt)Sn phases, in addition to (Ni,Au)\textsubscript{3}Sn\textsubscript{2} within groups B–D. The formation of the interfacial (Ni,Au)\textsubscript{3}Sn\textsubscript{2} phase is well in line with the thermodynamic assessment of Au–Ni–Sn ternary system at 320 °C [30], as represented with an isothermal section in Fig. 5. A contact line (CL) is drawn in Fig. 5 from nickel to AuSn alloy, whose composition 76.2Au\textsubscript{23.8}Sn (at-%) is calculated based on the original Au/Sn thickness ratio of 4:2 µm. During the bonding process, the 200-nm-thick nickel layer completely dissolves into the AuSn alloy composed of Liq+Hcp phases. The estimated nominal composition, when Au, Sn, and Ni layers have completely mixed at 320 °C, is marked in Fig. 5. The measured average gold solubility of 19 at-% in (Ni,Au)\textsubscript{3}Sn\textsubscript{2} is well in line with the thermodynamic data, as indicated in Fig. 5 by point P in the apex of three-phase triangle.

The device wafer side microstructure was designed based on the existing thermodynamic data [25]. The isothermal section of Au–Pt–Sn system at the bonding temperature is presented in Fig. 6. The platinum is assumed to dissolve completely into the liquid AuSn during bonding, and the nominal composition of the bond changes along the CL toward Pt. The nominal compositions with different platinum thicknesses are superimposed in the isothermal section by black points. After the bonding process, the platinum is mainly dissolved into the (Au,Pt)Sn phase, and the Hcp phase has transformed during cooling to the Au\textsubscript{5}Sn.

In order to reason the effect of dissolved Pt into the solidification and remelting temperature, an isopleth along the CL from the original AuSn alloy to pure Pt is calculated, and it is presented in Fig. 7. By fixing the composition, one can also derive the relative amount of phases (NP diagrams), and these are illustrated for both platinum thicknesses [Fig. 8(a) for 100-nm Pt and Fig. 8(b) for 200-nm Pt]. In the case of NP diagrams, it is assumed that the platinum layer dissolves...
Fig. 7. Isopleth of Au76.2Sn23.8 to 10 at-% platinum. The orange thick line illustrates the bonding temperature (320 °C), the blue dashed lines indicate the nominal compositions, and the yellow dashed line demonstrates the lowest temperature where liquid exists. Reaction paths 1 and 2 are marked for complete dissolution of 100- and 200-nm-thick platinum layers during bonding and solidification during cooling, respectively.

Fig. 8. NP diagrams of Au–Sn/Pt bonds with platinum thickness of (a) 100 and (b) 200 nm. Black dashed line illustrates the bonding temperature. Completely and distributes uniformly into the AuSn bond; thus, the concentrations of 2.1 at-% and 4.1 at-% are expected with 100- and 200-nm-thick platinum layers, respectively.

In the case of 100-nm-thick Pt layer, there is liquid, AuSn[Pt], and Hcp phases in equilibrium at the bonding temperature (320 °C), and the structure solidifies at ~300 °C with AuSn[Pt]+Hcp structure [see reaction path 1 in Fig. 7 and amount of liquid in Fig. 8(a)]. During cooling, the Hcp phase transforms to the Au5Sn phase. With the 200-nm-thick Pt metallization, there are only AuSn[Pt] and Hcp phases existing at 320 °C; thus, the bond solidifies isothermally during bonding [reaction path 2 in Fig. 7 and amount of phases in Fig. 8(b)]. Similar to the thinner Pt metallization, the Hcp phase converts to the Au5Sn phase during cooling.

When we consider subsequent heating of the bonds at following processing such as getter activation or assembly steps, based on the modeled solidus line in Fig. 7, the mushy zone starts at ~352 °C with 200 nm (4.1 at-%) Pt. The peritectic reaction temperature is at 378.5 °C, which could be achieved by increasing the platinum thickness to ~300 nm.

The solidus temperature of the bond is expected to rise from ~300 °C to above 350 °C with thicker platinum. This offers a promising feature to the bonded wafers for further manufacturing processes such as getter activation without entering the mushy zone of the bond. Katz et al. [21] reported a rise in the remelting temperature (from 280 °C to ~370 °C) of the Au–Sn eutectic solder after dissolution of 200-nm-thick Pt metallization into 2.25-µm-thick solder. The benefit of the Au–Pt–Sn system compared to the binary eutectic AuSn is that even a minor dissolution of Pt into the AuSn phase increases the melting point of the system, and thus, the remelting temperature of the bond is increased with a lesser amount of gold. In order to achieve remelting temperature of 350 °C, the amount of gold needs to be doubled. In addition, even the effect of nickel was excluded from the Au–Pt–Sn analysis above, the formation of the (Ni,Au)3Sn2 phase consumes tin (more than gold) from the Au–Sn/Pt stack. Thus, it is assumed that the solidus and liquidus temperatures are actually even slightly higher than estimated without the effect of cap wafer side metallizations. All the results highlight the benefit of thermodynamic data utilization and visualization: Metallizations can be easily designed in order to achieve the desired microstructure.

C. Shear and Tensile Test Results

Shear test results are presented in Fig. 9, and tensile test results are gathered into Fig. 10. Sample groups were tested...
with the Welch’s t-test ($\alpha = 0.05$) in order to clarify which dissimilarities were significant. The $p$-values of the differences are presented in Tables I and II. Within as-bonded samples, group D had the highest shear and tensile strength. The shear strength did not significantly differ between groups C and D, but the tensile strength of group C was considerably lower than D. Based on the results, there was no difference in mechanical strength between groups A and B.

There were no substantial changes in the strength observed after the HTS test. The statistically significant drop in strength with group C samples after the TS test can be explained with the cracks that were detected in the cross-sectional analysis. In order to explain the observed differences in mechanical strength, a fracture surface analysis was performed.

D. Fracture Surface Analysis

In this section, the identified fracture modes are presented first, and then their distribution per test group is evaluated. Fracture modes for different groups are summarized in Fig. 11(a).

Mode Ia presents the interfacial failure between the TiW adhesion layer and the Au$_5$Sn phase. It also includes interfacial failure between SiO$_2$ and TiW, as well as cohesive failure in SiO$_2$ [see red dashed line in Fig. 11(a)]. The fracture mode Ib is marked as an interfacial failure between TiW and (Ni,Au)$_3$Sn$_2$ [including also the TiW/SiO$_2$ failures; see Fig. 11(a) light blue dashed lines]. Thus, in general, mode I refers to the cap wafer side interfacial failure.

Fracture mode II is assigned for cohesive fracture of the bond [see dark blue dashed line in Fig. 11(a)]. Mode IIIa fractures are observed as an interfacial failure between the (Au,Pt)Sn phase and the Au$_4$Ti[Sn] phase, Au$_4$Ti[Sn] and underlying metallization, as well as cohesive fractures in the SiO$_2$/Ti/Mo layers [see purple dashed line in Fig. 11(a)]. In group C, in which the molybdenum was omitted, this failure was correspondingly marked as a fracture mode IIIb [see brown dashed line in Fig. 11(a)]. The observed fracture modes are also illustrated on the fracture surface images in Fig. 11(b)–(e).

In Figs. 12 and 13, the distribution of different fracture modes in the shear and tensile tests is presented, respectively. Group A exhibited interfacial failure between TiW adhesion layer and the Au$_5$Sn phase (mode Ia). The main fracture mode within groups B and D was Ib, the second most common fracture mode was II, and some mode IIIa fractures were observed as well. Group C had the same fracture modes as groups B and D. However, as the molybdenum layer was not deposited in this group, interfacial failures at the device wafer side are mode IIIb. Fracture mode distributions revealed...
Omitting the molybdenum from the device wafer side did not seem to have clear strengthening effect than previously shown in [6] or in die attachment applications utilizing a nickel barrier under Au–Sn solder [13], [21]. On the other hand, even though there are no statistical differences in the mechanical strength between groups A and B, implementation of nickel as a buffer layer changes the failure mechanism slightly. The stress distribution and failure initiation may vary between wafer-to-wafer bonds as well as with unsymmetrical metallizations on cap and device wafers. Strength values measured for groups A and B do not drastically differ from Au–Sn SLID bonds in [6].

**IV. Conclusion**

Based on the results obtained in this paper, the following conclusions and design rules can be summarized.

1. **High-strength and thermally stable AuSn/Pt SLID bonds** were achieved and optimized for wafer-level process integration of MEMS manufacturing. The platinum was consumed in the formation of IMCs, mainly dissolving into the (Au,Pt)Sn phase.

2. The metallization layers were designed, and platinum thickness was optimized based on the thermodynamic data in order to achieve microstructure having a high remelting temperature and mechanical strength.

3. The molybdenum layer below the Pt metallization increased the tensile strength of the Au–Sn/Pt SLID bond and prevented cracking under the TS test.

4. A thicker platinum layer (200 versus 100 nm) increased the strength of the bond and the solidus temperature. Increased shear strength was observed as a higher fraction of cohesive failures in fracture surface analysis.

When both shear and tensile tests are utilized, detailed mechanical reliability information about the compatibility of the interconnection materials is obtained. Overall, AuSn/Pt SLID bonding offers an interesting possibility for hermetic sealing and electrical interconnections on different types of wafers for the MEMS manufacturing and 3-D integration platform.

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