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A Low-Power Hardware Stack for Continuous Data Streaming from Telemetry Implants

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***Abstract*—This paper describes the hardware implementation of a custom communication protocol tailored for low-power telemetry data streaming over an inductive link. The application-specific features of typical RFID implementations such as random number generation and variable data rate support are omitted from the proposed implementation, focusing only on the continuous data transfer. The post-synthesis results of proposed communication scheme implemented on 28nm CMOS FDSOI process show power consumption of 3.11 μW while running from a 845.7 kHz clock and occupying 0.0048 mm^2 of die area. The current implementation provides an uplink rate of 8 kbit/s, sufficient for streaming of 1-channel 1 kHz 12-bit sample recording.**

I. Introduction

WIRELESS data transmission capability over an inductive [1] or acoustic link [2] is a de-facto standard for implantable biomedical systems. Modern subcutaneous implants are designed to operate solely on DC power extracted through the same inductive link [3], [4], making the magnetically-coupled coils an essential part of the reader-implant interface. Being in a low-power device, telemetry implant still requires fast and resilient uplink channel in order to reliably transmit the data acquired at the front end. The uplink bit rate and the power consumption can be considered as the key design specifications for the communication system of an implant [5]. In addition, error detection and correction are indispensable for a communication protocol targeted at transmission over a lossy and noisy medium such as skin tissue.

A standard implementation of a Radio-Frequency Identification (RFID) processor has a set of communication primitives namely, donwlink decoder, uplink encoder, and state control together with additional protocol-specific features such as random-number generation [6] and encryption [7] which may not be necessary in context of a low-power sensor implant. The design of a transceiver for sensor implants can do away with such overheads to obtain a power efficient yet robust communication link.

In this paper we present an uplink-intensive communication stack which provides the means to communicate with an external reader device and mitigate data loss. The paper is organized as follows. Section II introduces the key properties of the proposed communication scheme. Section III describes the implementation of the scheme in digital logic and Section IV presents the results of hardware synthesis. The conclusions will be given in Section V.

II. Proposed Communication Scheme

This section describes the requirements on a communication system that needs to acquire a continuous stream of data and introduces the key properties of the proposed communication scheme.

A. Buffering and Error Mitigation

In context of telemetry implants, the data payload often comes as an uniformly sampled signal. The task of the communication subsystem, especially in implants without storage is to ensure that all the data arrives at the reader device. In order to preserve the order and integrity of the sampled sequence transmitted through a noisy medium, the communicating entities must incorporate a mechanism to avoid data loss and corruption. Two necessary protocol features required for this are the error detection and the acknowledgment procedure [8]. When the error cannot be corrected, the received samples shall be stored in buffer memory for retransmission. The data can be discarded from the buffer only after the receiving acknowledgment from the reader.

B. Communication System Architecture

The Amplitude-Shift Keying (ASK) and backscattering are considered to be techniques of choice in context of low-power inductive implants [9], [10]. In proposed communication scheme, the downlink commands are sent with Pulse-Width Modulated (PWM) ASK and the implant response is backscattered to the reader with an On-Off Keying (OOK) sequence encoded with FM0 [11]. As a generic convention on PWM, the Pulse-Interval Encoding (PIE) is used [11]. Fig. 1 illustrates a typical reader-implant interaction.

To avoid data loss, the minimum set of streaming functionality outlined in section II-A is implemented along with communication primitives. Fig. 2 shows the structure of the communication system. For the communication clock frequencies are considered that are derivable from a 866 MHz carrier Ultra-high frequency (UHF) RFID band allocation in Finland [12]. As a solution for transferring the data from the sampling clock domain, the asynchronous first-in first-out (FIFO) model is utilized as the uplink buffer. The error

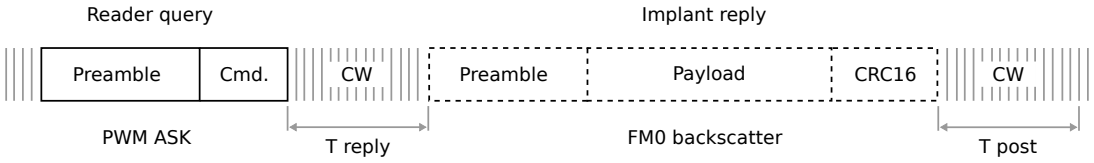

Fig. 1. Communication between the reader and the implant. CW stands for continuous wave emitted by the reader. The reader query is amplitude modulated while implant reply is transmitted using backscatter modulation (dashed line). The periods of transmission by reader and implant are followed by delays of T_{reply} and T_{post} accordingly.

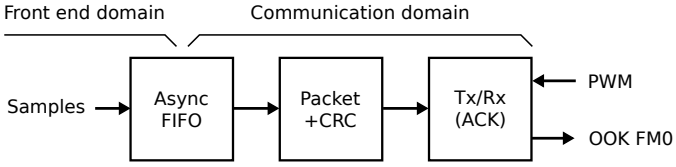

Fig. 2. Structure of the communication system.

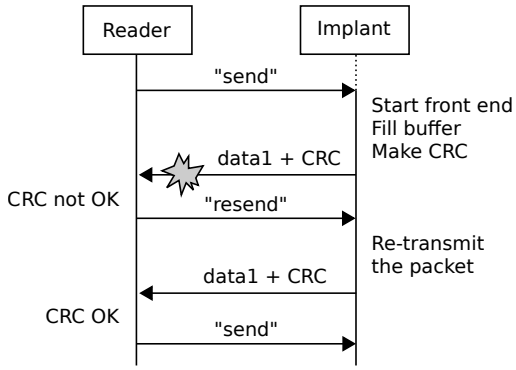

Fig. 3. Example communication scenario. Reader requests the previous packet in case CRC recovery fails.

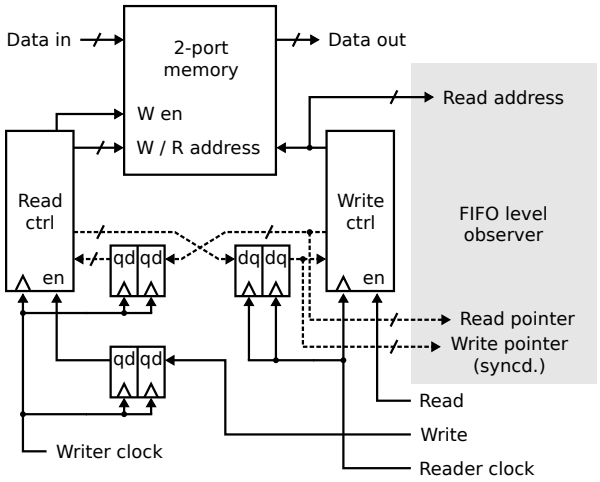

Fig. 4. Asynchronous FIFO with a level observer. The reader handles both ends of the queue via synchronized one-bit line. The dashed lines denote the gray-coded pointer data.

detection is realized by padding the packet with a Cyclic Redundancy Check (CRC) pattern, allowing for recovery of 1-bit payload errors at the receiver [13], [14]. The acknowledgment logic (ACK) is implemented as a part of the transceiver state machine. A minimalistic acknowledgment procedure is formulated with two reader commands, namely "send" and "resend". The former instruction is issued for both requesting the new data and approving the previous transmission. When transmission fails, the last packet is requested instead with the "resend" instruction as shown in Fig. 3.

To reduce the design footprint, the proposed implementation utilizes only protocol features that are relevant for data transmission between the implant and the reader. Functionalities such as support for variable data rate and memory operations commonly present in RFID processor designs [6], [15], are excluded, optimizing this communication scheme specifically for wireless data streaming.

III. Implementation

This section describes the implementation of the proposed communication scheme in digital hardware and substantiates the decisions made during the design process.

A. Asynchronous FIFO Buffer

The access to the state of the data buffer is crucial for timely transmission of accumulated readings. The state of an asynchronous FIFO is represented by read and write pointers and is distributed across separate clock domains and needs to be re-synchronized after each event [16]. Fig. 4 shows the structure of an asynchronous FIFO with the level observer. The level observer logic determines the amount of words in the buffer based on the information obtained from the read control unit. The FIFO level is found with binary subtraction between read and write addresses and the full condition is resolved by pointer comparison [16]. In order to avoid losing samples at the input of the buffer, it is mandatory to dispatch the data sooner than FIFO becomes full. The synchronization of the read pointer lasts two cycles of the sampling clock, causing a delay in removing the "full" condition at the reader side. As a requirement, the FIFO capacity should be strictly larger than the payload size to be read from the buffer.

In this work, a 8-word deep FIFO is utilized to store 12-bit samples arriving at 1 kHz. The threshold of packet manager is two samples per payload, which ensures that the data is flushed before the FIFO is full. The selected buffer depth

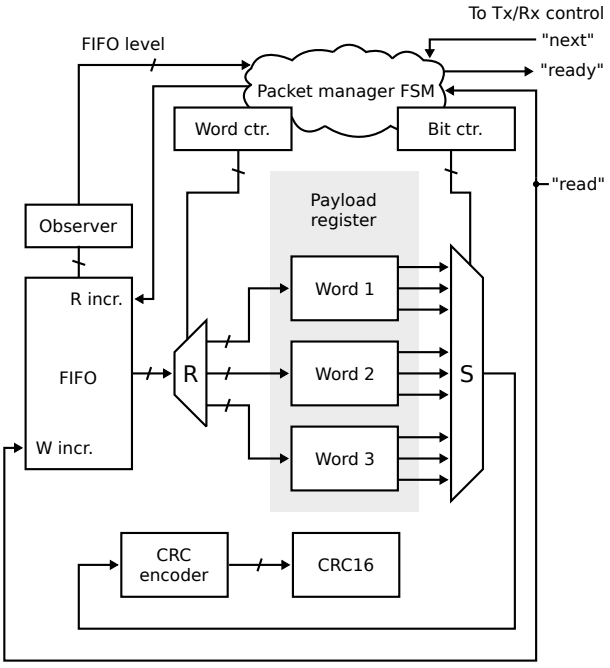

Fig. 5. Packet manager module. The registers which store payload and CRC are further accessible for the transceiver.

allows up to 7 ms (i.e. 7 samples in memory) of delay due to retransmission.

B. Communication Packet Manager

The packet manager provides the transceiver with the uplink data by populating the payload from the buffer and appending it with the CRC checksum. The structure of the packet manager module is shown in Fig. 5. The difference between sampling and communication clock domains provides enough time in between samples to use a serial-type CRC encoder [17], thus allowing to further minimize the physical area of the system [18]. The packet manager FSM is controlling the packet assembly process according to state diagram shown in Fig. 6. Once enough samples are accumulated in the buffer, the payload register is rewritten with a number of consecutive samples from the FIFO through the routing (R) demultiplexer. The contents of the new payload are serialized into the CRC encoder with the serializer (S) multiplexer.

C. Transceiver

The transceiver control is distributed between two state machines, namely the Transceiver FSM and the PWM decoder FSM, as shown on Fig. 7. The PWM sampling resolution is the most restricting factor for the transceiver clock rate [6]. Since the variable data rate support is excluded in this implementation (section II-B), the downlink PWM time constants are fixed at values listed in table I. The selection of such coarse downlink constants allows to run the transceiver clock as slow as 845.7 kHz (derived from carrier) further reducing the dynamic power consumption of the system. In order to keep the backscattering frequency within limits specified in the EPC RFID C1 G2 [11], the FM0 uplink rate is set to 422.85 kHz. The transceiver generates uplink clock with a

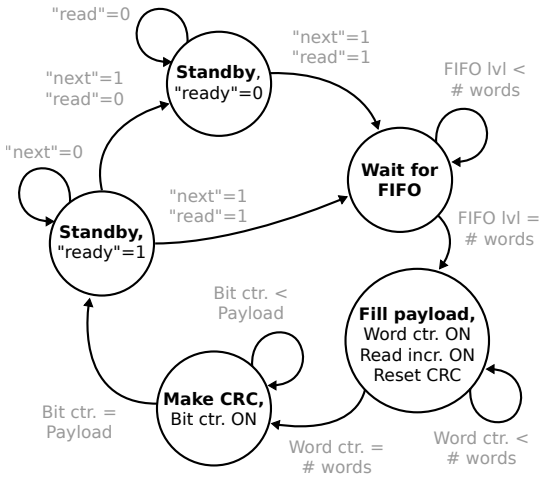

Fig. 6. Packet manager state diagram

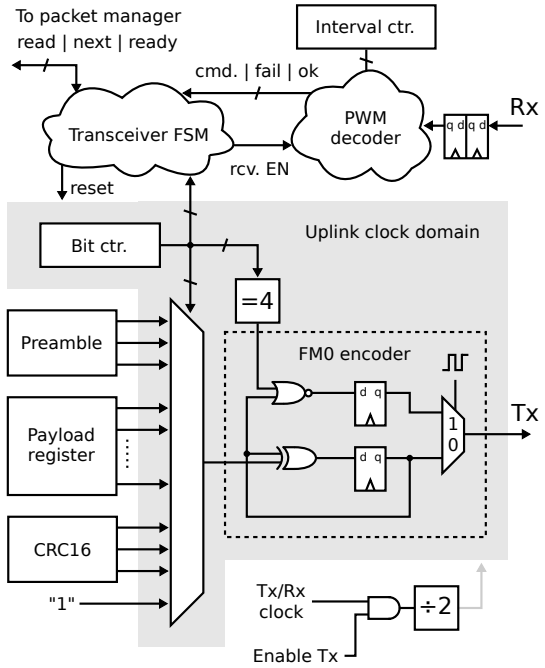

Fig. 7. Transciever structure

TABLE I
COMMUNICATION TIME CONSTANTS

Wait Periods	
Treply	40 μs
Tpost	40 μs
PWM Parameters [11]	
Delimiter	12.5 μs
data-0	15 μs
data-1	25 μs
PW	5 μs
RTcal	40 μs

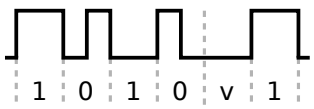

Fig. 8. FM0 preamble. The intentional encoding violation "v" is used to aid the frame synchronization.

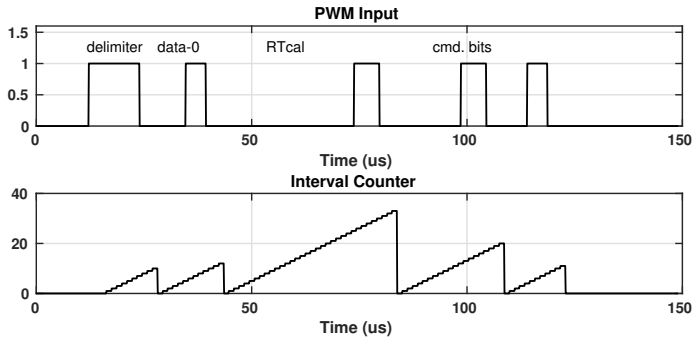

Fig. 9. Value of the Interval counter during the decoding of command from the reader.

divider, providing a phase-coherent subdomain for safe register comparisons at the FSM side. The packet is serialized into the FM0 encoder as shown in Fig. 7. This 2-flipflop encoder structure is derived from the FM0 state transition diagram [19]. The NOR gate suppresses the output of the encoder for the next high cycle of the uplink clock, producing the desired encoding violation during the transmission of FM0 preamble symbols "101001" as shown in Fig. 8. At the end of the packet, a dummy "1" is appended to indicate the end of FM0 signaling [11].

D. PWM Decoding

The PWM decoder is built as an FSM which utilizes a fast Interval counter to measure the incoming symbols. The state transitions are tailored such that the counter value is compared against the pre-defined interval values and then reset for the new measurement. Fig. 9 shows the behaviour of the Interval counter during the decoding.

E. Transceiver FSM

The transceiver FSM implements the proposed communication protocol as shown in flowchart on Fig. 10. Mandatory delay intervals T_{reply} and T_{post} are measured with a dedicated delay counter (not on Fig. 7). In order to control the state of implant transceiver, an exclusive "session" bit in transceiver memory is set or reset with commands "send" and "stop" respectively. Initialized with zero, this flag controls the writing into FIFO as the "read" input to the packet manager.

IV. Results

This section presents the evaluation of the design by means of hardware synthesis and simulations.

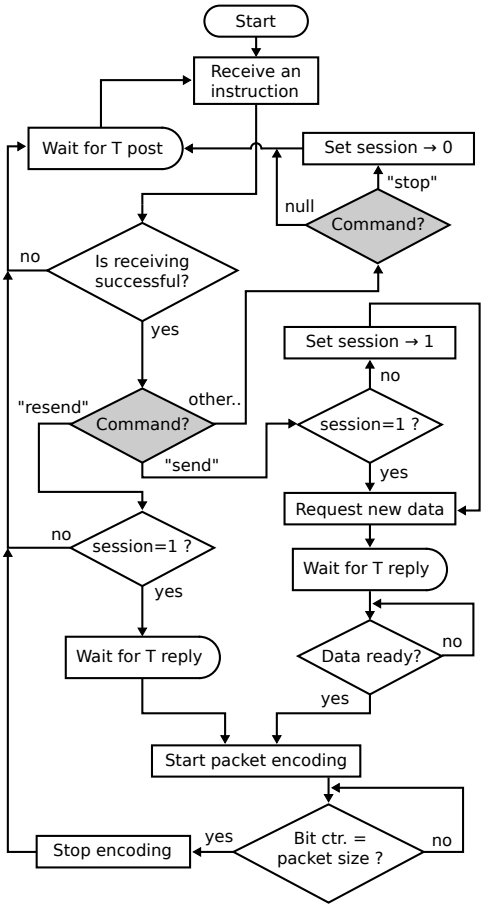

Fig. 10. Flowchart of the Transceiver FSM operation. Gray blocks indicate decisions based on the command from the reader.

A. Hardware Synthesis

The hardware description of the proposed communication system was implemented in VHDL and synthesized for CMOS 28nm FD-SOI process using Synopsis Design Compiler. The layout of the digital circuit is done in Cadence Innovus. The timing of implemented design is verified by Synopsis Prime Time static timing analysis (STA) tool. The functionality of the communication system is tested using behavioural simulation with back-annotated delays extracted from the layout.

B. Behavioural Simulation

Figure 11 demonstrates the operation of the implemented system as it communicates with the reader emulator. Upon reader request, the implant accumulates the incoming data and dispatches it shortly. The reader acknowledges the successful transmission by requesting new data, and the procedure repeats. Upon issuing the "resend" command continuously, the reader forces the implant to reuse the packet while accumulating the data in FIFO. After the reader starts acknowledging the incoming packets again, the implant will continue the communication by dispatching all of the FIFO entries first.

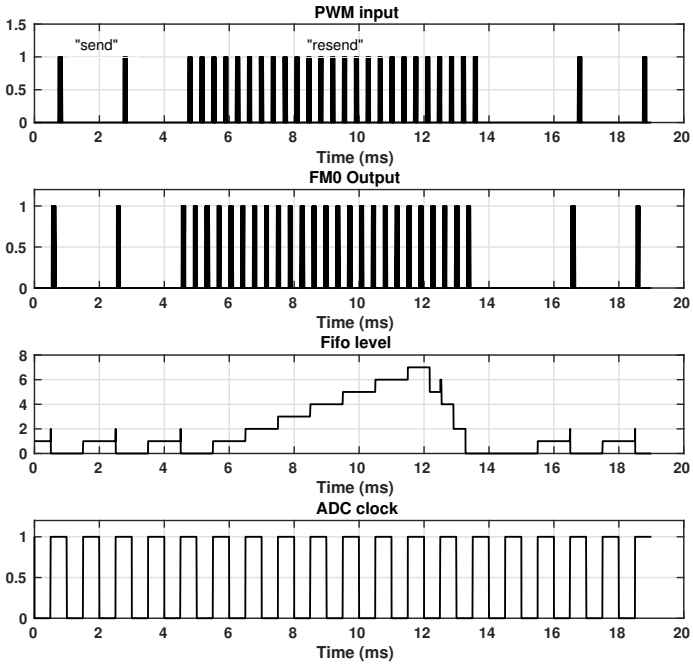

Fig. 11. Simulation of data loss and retransmission.

C. Power and Area

The average power consumption of the system is estimated with a transient simulation of a synthesized netlist. The simulation reconstructs the typical transceiver activity during active communication. Table II shows the relevant statistics.

TABLE II
POST-SYNTHESIS RESULTS

Technology	CMOS 28nm FD-SOI
Supply voltage	0.7 V
Transceiver clock	845.7 kHz
Uplink rate	8 kbit/s
Area	0.0048 mm^2
Average power	3.11 μW
Leakage power	2.7 μW

V. CONCLUSION

This is a custom implementation of inductive link communication protocol especially targeted for telemetry data transfer in the context of implants. The proposed communication scheme provides the means to communicate with an external reader and mitigate data loss while utilizing minimal hardware resources. The design target was achieved by incorporating only the functionality which is necessary for reliable data transmission.

The post-synthesis simulation shows power consumption of 3.11 μW at clock rate of 845.7 kHz and supply of 0.7 V. The achieved layout area is 0.0048 mm^2. The uplink rate of 8 kbit/s is sufficient for transmission of 1-channel 1 kHz 12-bit sample, and up to 7 ms time is allowed for retransmission during channel failures.

The power consumption estimates of indicate that the proposed hardware implementation fits well in the implant power budget down to 1 mW [20], leaving sufficient energy resource for the signal acquisition front-end.

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