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A VCO-Based ADC with Relaxation Oscillator for Biomedical Applications

A VCO-based ADC with Relaxation Oscillator for Biomedical Applications

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Abstract—This paper describes a voltage controlled oscillator (VCO) -based ADC for biomedical applications which employs a relaxation oscillator for voltage-to-frequency conversion. The proposed circuit uses a redundant pair of capacitors to mitigate the conversion error resulting from the time required for resetting the capacitor. A switch matrix with feedback helps sustain oscillations. Further, the VCO frequency approaches zero as the input voltage approaches zero unlike a converter with ring oscillator, thereby reducing power consumption. Post-layout simulation of the proposed ADC designed with a 28 nm FDSOI CMOS technology shows an ENOB of 8 and power consumption of 12 μW from a 0.7 V supply.

I. INTRODUCTION

Real-time measurement of physiological signals from the human body is useful in prevention, diagnosis and treatment of diseases. In addition, there is growing need of integrated electronics for monitoring physiological signals as medical advancement evolves into personalized health-care. Hence, the design of integrated electronics for biomedical applications helps advance medical research and the development of closed-loop solutions such as brain-machine interfaces for prostheics control [1].

Biomedical integrated electronics that are implanted in the human body are typically limited by the power that can be delivered to the implant. The limited power available to implantable biomedical electronics sets the low power requirement in the design of internal sub-systems. One of the main sub-system in the design of implantable biomedical electronics is the analog front-end (AFE) which consists of signal acquisition and analog-to-digital conversion (ADC) modules. There are several low-power analog front-end designs based on successive-approximation register (SAR) and delta-sigma ADC structures that are widely used in biomedical applications [2], [3]. In this paper, we propose an alternate time-based ADC architecture with moderate power consumption targeted towards biomedical applications.

Time-based analog-to-digital converters are gaining popularity in low-power applications as process and device features (gate length and supply voltage) reduce due to scaling in technology nodes [4]. Faster processes increase the effective time resolution that can be achieved, while amplitude resolution and power consumption are decreasing with the steady decrease in supply voltages. Low-power time-based ADCs can be realized using ring oscillators. Ring oscillators are simple, robust, scalable, power efficient and require small area. Ring oscillator based ADCs also demonstrate inherent first-order shaping of quantization noise and sinc-type filtering. These features of
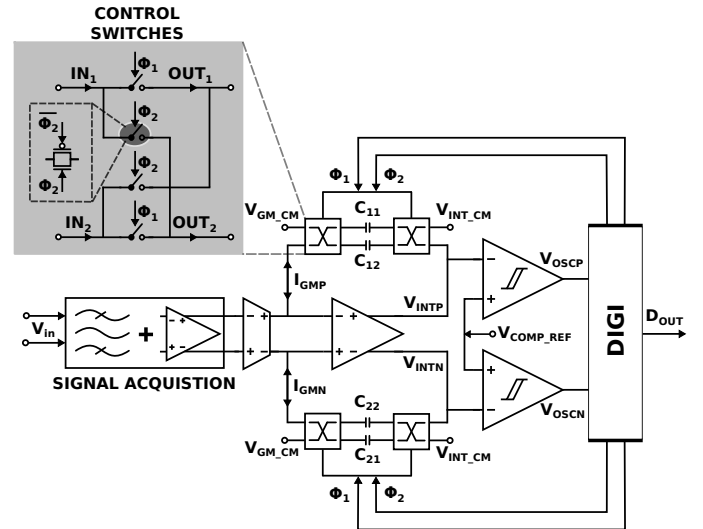

Fig. 1. The proposed relaxation oscillator based ADC.

ring oscillator based ADCs alleviate the requirements for noise and filtering performance of the system, which is especially beneficial in the 1/f-noise dominated low frequencies of bio-potential signals [4].

The drawback of ring oscillator based ADCs is the poor linearity of the voltage-to-frequency (V-F) conversion which limits the achievable effective number of bits (ENOB) [5], [6]. As a result, additional calibration and linearization techniques are required to further improve the effective resolution of ring oscillator based converters [7], [8]. These linearization techniques increase the complexity and power consumption of ring oscillator based converters. In contrast to ring oscillators, relaxation oscillators are commonly used in frequency references due to their relatively stable and linear oscillation frequency range [9], [10].

In this paper, we investigate the use of a relaxation oscillator as an alternative to ring oscillator in the design of the proposed VCO-based ADC in Fig. 1. Post-layout simulation results show that the proposed ADC achieves an ENOB of 8 with sampling rate (F_s) of 10 kSPs, while consuming 12 μW of power in continuous operation from 0.7 V supply. The rest of the paper is organized as follows. Section II describes the operation of the proposed circuit. Section III presents simulation results and Section IV summarizes the performance of the ADC.
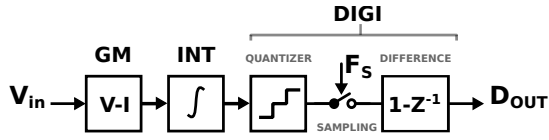
Fig. 2. Simplified model of the system.

Fig. 3. Timing of the integrating capacitors and control switches.

II. OPERATION PRINCIPLE

The low-frequency and small amplitude signal characteristics of bio-potentials determine the main design requirements of the analog-to-digital converter. The proposed architecture of the relaxation oscillator based ADC is presented in Fig. 1. The bio-potential signal acquisition process consists of a band pass filter and an amplifier stage for limiting the signal bandwidth and amplifying the signal in preparation for further processing by subsequent stages. The acquired and amplified input voltage signal (V_{in}) is converted to current signal by the transconductance (GM) stage.

The relaxation oscillator consists of integrating capacitors that are charged and discharged with the currents from the GM-stage. Hence, the frequency of the oscillator changes with the current from the GM-stage. Lastly, the integrating capacitors are reset by the cross switch controls from the digital logic (DIGI) block based on the pulses from the oscillator. The combined system comprises of a low-noise amplifying band-pass filter (BPF), voltage-to-current transconductance-stage, a high gain integration stage (INT), fast comparators for quantization (COMP) and finally the digital logic to control the integration control switches and generation of the digital output codes (D_{OUT}). A simplified model of the single-ended operation of the system is presented in Fig. 2.

A. Oscillator switching scheme

This section describes the switching process and how oscillation is achieved in the proposed circuit. The oscillator frequency is controlled by the set (charging) and reset (discharging) times of the integration control switches. Hence, the integration control switches play an important role in the operation and performance of the relaxation oscillator. The output currents from the GM-stage (I_{GMP}, I_{GMN}) are sampled into the integrating capacitors that are reset by the integration control switches. Fig. 3 illustrates how the four integrating capacitors (C_{11}, C_{12}, C_{21}, C_{22}) are charged and discharged based on the switch control phases (ϕ_1 and ϕ_2).

The oscillation is achieved by alternating between the integrating capacitor pairs that are charged/discharged based on the switch control phases (ϕ_1 and ϕ_2). The switch control phase ϕ_1 is complementary to phase ϕ_2. There are two pairs of capacitors connected to the integrator as shown in Fig.1: C_{11} paired with C_{21}, and C_{12} paired with C_{22}. The first pair (C_{11} and C_{21}) is connected in feedback to the differential inputs and outputs of the integrator during phase ϕ_1, while the second pair (C_{12} and C_{22}) is connected to the common-mode voltages (V_{GM_CM} and V_{INT_CM}) during the same phase. When the integrator output voltages (V_{INTP} and V_{INTN}) reach the comparator threshold, the control phases (ϕ_1 and ϕ_2) are flipped by the DIGI logic and the integrating capacitor pairs are swapped. This implies that the (C_{12} and C_{22}) pair that was previously held at common-mode voltages is connected in feedback to the integrator during phase ϕ_2, while the other pair
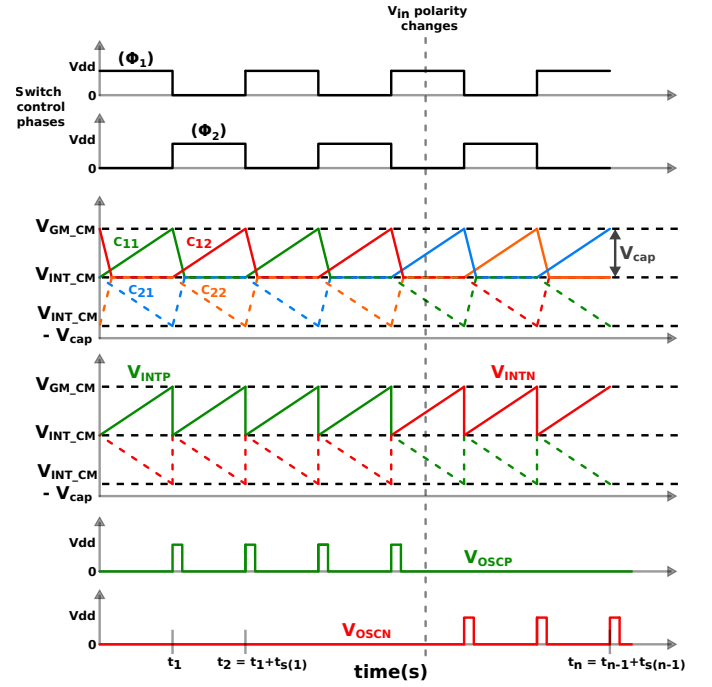
(C_{11} and C_{21}) is held at common-mode voltages. This pattern repeats in similar fashion until the polarity of the GM output currents (I_{GMP}, I_{GMN}) changes during each half-cycle of the input signal. Then, the charging and discharging patterns of the integrating capacitor pairs are reversed as observed in Fig. 3.

In addition, the oscillator output pulses are controlled in a bi-phasic manner based on the input voltage polarity change. Hence, only one oscillator output is active during each half-cycle of the input signal. The active oscillator output (V_{OSCP}, V_{OSCN}) is determined by the integrator output (V_{INTP}, V_{INTN}) that crosses the comparator threshold. The hysteresis comparator threshold level is defined by the comparator reference voltage (V_{COMP_REF}) and the internal hysteresis voltage of the comparator (V_{COMP_HYST}). Thus, one of the common voltage levels for the control switches is (V_{GM_CM}), which is designed to be the sum of V_{COMP_REF} and V_{COMP_HYST} voltages. This allows the integrating capacitor pair that is connected in feedback to the integrator to be charged from V_{INT_CM} to V_{GM_CM} voltage. The difference between V_{INT_CM} and V_{GM_CM} defines the voltage over the integrating capacitors (V_{cap}).

The developed switching scheme ensures reliable oscillation without the need for a constant operating or reference frequency. Unlike in ring oscillator based ADCs, the proposed ADC outputs zero pulses (i.e zero frequency) with zero input voltage, which reduces dynamic power consumption and eliminates the need for separate oscillator bias voltage or current source. In addition, swapping the charged/discharged capacitor pair reduces the conversion error from the delay associated with discharging a single capacitor in each feedback path of the integrator when compared with other relaxation oscillator implementations [11], [12].

The proposed circuit also preserves the first-order noise shaping and sinc-type filtering features that are present in ring oscillator based ADCs. The noise-shaping feature is

achieved in the DIGI module by counting pulses from each oscillator output, sampling the accumulated counter codes and performing a difference operation between sampled counter codes as presented in Fig. 2. The sum of the digital codes from both oscillator outputs (V_{OSCP} and V_{OSCN}) corresponds to the input voltage (V_{in}).

Furthermore, the proposed relaxation oscillator implementation of VCO-based ADC exhibits an improved voltage-to-frequency conversion linearity over ring-oscillator based ADCs due to the use of an amplifier in feedback, which translates the linearization challenge to gain maximization challenge. On the other hand, ring oscillators usually do not have similar feedback mechanism and thus suffer from nonlinear voltage-to-frequency transfer characteristics.

B. Voltage-to-Frequency Conversion Theory

The ideal transfer function for the voltage-to-frequency (V-F) conversion of the proposed circuit can be derived from the integration time required for each integrator output voltage (V_{INTP}, V_{INTN}) to reach the comparator threshold voltage, as the capacitor $C = C_{11,21,12,22}$ is charged with a varying output current ($I_{GM}(t) = G_m V_{in}(t)$) from the GM-stage:

$$t_s(t) = \int_0^{V_{cap}} \frac{C}{G_m V_{in}(t)} dV = \frac{C V_{cap}}{G_m V_{in}(t)} \qquad (1)$$

$$= \frac{C V_{cap}}{I_{GM}(t)} = R_{eq} C \qquad (2)$$

where the varying input voltage signal is V_{in}, which is converted to current with transconductance G_m and V_{cap} is the voltage over the capacitor when each capacitor C is charged from V_{INT_CM} to V_{GM_CM}. In addition, R_{eq} is the equivalent resistance from V_{cap}/I_{GM} and the oscillator output frequency $f_{osc}(t)$ is the inverse of the varying integration time $t_s(t)$. Hence, equation (3) represents a general notation of the voltage-to-frequency conversion for a varying input voltage $V_{in}(t)$, where $K_{osc} = G_m/V_{cap}C$ is the V-F conversion gain of the relaxation oscillator.

$$f_{osc}(t) = \frac{1}{t_s(t)} = \frac{G_m V_{in}(t)}{V_{cap} C} = K_{osc} V_{in}(t) \qquad (3)$$

The resolution of the digital output codes (D_{OUT}) is determined by the maximum amount of pulses that the oscillator can generate within a defined sampling period. The amount of pulses that can be generated with a given input voltage is proportional to K_{osc}. This implies that K_{osc} should be maximized in order to increase the accuracy of V-F conversion by ensuring that:

- Voltage over capacitor V_{cap} is minimized.

- Integration capacitances C are minimized.

- Transconductance G_m is maximized.

The presented V-F conversion theory shows that the input voltage to oscillator output frequency conversion should be ideally linear based on equation (3). This suggests that possible sources of non-linearity in the proposed circuit are in the implementation of the functional blocks and control switches.

III. POST-LAYOUT SIMULATION RESULTS

The proposed relaxation oscillator based analog-to-digital converter was implemented in 28 nm FDSOI process and Fig. 4 shows the layout of the chip. The prototype chip is a bio-potential measurement sensor interface which includes the analog front-end, energy harvesting, and digital signal processing (DIGI) modules. The analog front-end consists of the band-pass filter amplifying stage for signal acquisition and the relaxation oscillator based ADC.
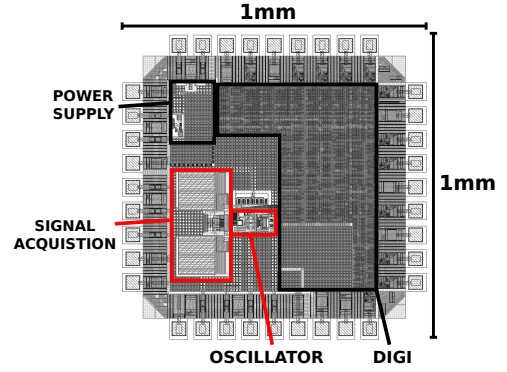

Fig. 4. Layout of the design implemented in 28 nm FDSOI.

The oscillator output frequency as a function of input voltage is presented in Fig. 5. The slope of the transfer curve corresponds to the V-F conversion gain of the oscillator within 1 mV input range. Fig. 5 also shows that the oscillator frequency is zero when the input voltage is zero. This feature in the proposed circuit allows implementation of power-cycling techniques when used in biomedical applications for achieving more power savings over time and less energy consumption.
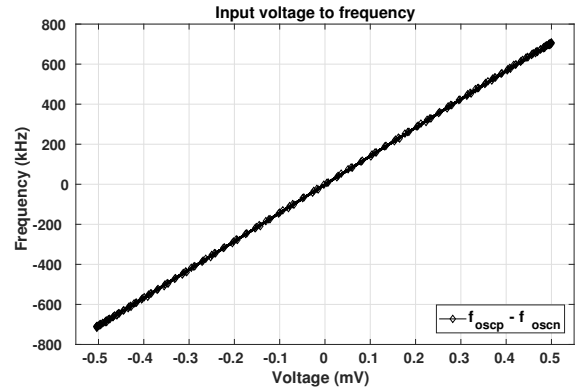

Fig. 5. Oscillator frequency range over 1 mV input voltage range.

Fig. 6 presents the bi-phasic control of the oscillator outputs as earlier discussed in section II. The positive oscillator output (V_{OSCP}) is active during the positive half of the input voltage V_{in} while the negative oscillator output (V_{OSCN}) is active during the negative half of the input voltage as observed in Fig. 6. Hence, the dynamic power consumption of the oscillator pulse counters in the DIGI module is reduced by controlling the active oscillator output in a bi-phasic fashion.

The dynamic performance of the analog-to-digital converter was evaluated using a 1 mV peak-to-peak (pp) sinusoidal signal with 157 Hz frequency targeted towards bio-potential
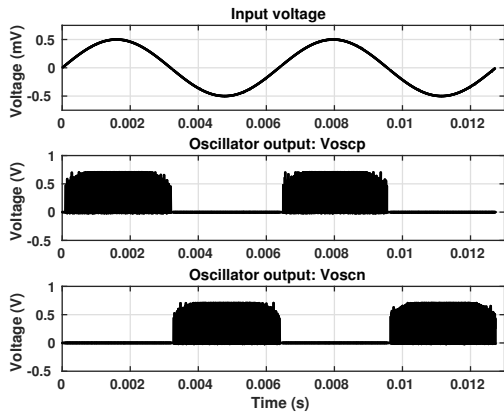
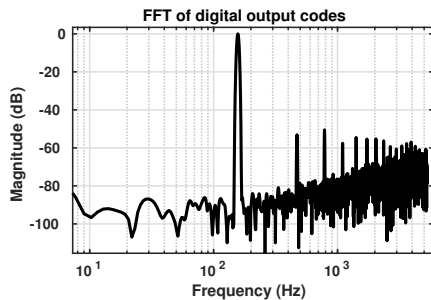Fig. 6. Bi-phasic operation at the oscillator outputs.

Fig. 7. FFT of digital output codes from 157 Hz, 1 mVpp sine input.

TABLE I.   PERFORMANCE SUMMARY

Parameters	Values
Technology (CMOS)	28 nm FDSOI
Supply voltage	0.7 V
Input signal range	1 mVpp
Input bandwidth	500 Hz
Sampling rate	10 kHz
Oversampling ratio (OSR)	10
SNR	80 dB
SFDR	53 dB
ENOB	8 bits
Power consumption	12 μW

monitoring. The sampling rate of the quantizer is selected to be 10 kHz in order to present the main harmonics. The typical sampling rate of the system is 1 kHz but there is a need for oversampling in order to benefit from the noise-shaping feature of the ADC. Fig. 7 shows the spectrum of the digital output codes from the 157 Hz input signal. Without employing any calibration or linearization techniques, the spurious free dynamic range (SFDR) from the digital output codes is 53 dB and the signal-to-noise ratio (SNR) is approximately 80 dB within the signal bandwidth of 500 Hz.

Further analysis into the potential source of the odd-harmonic limited resolution indicates that the control switches on the GM output current paths significantly contributes to the V-F converter performance. Nonetheless, the achieved resolution is sufficient for bio-potential monitoring applications. A summary of the performance of the proposed relaxation oscillator based ADC is presented in Table I.

IV. CONCLUSION

In this paper, we present a VCO-based ADC that utilizes a relaxation oscillator as an alternative to ring oscillators for voltage-to-frequency conversion. The proposed ADC uses a switching scheme that ensures reliable oscillation without the need for a constant operating frequency from an additional reference source. In addition, the developed switching scheme minimizes the conversion error from the delay associated with discharging the integrating capacitors that are used in the relaxation oscillator. The proposed ADC also supports over-sampling and exhibits first order noise-shaping characteristics. By investigating the use of the proposed relaxation oscillator architecture in a VCO-based ADC, post-layout simulation results show that the ADC achieves power consumption of 12 μW from a 0.7 V supply and ENOB of 8 which is sufficient for the targeted application area.

V. ACKNOWLEDGMENTS

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