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A Zero-Crossing Approximation of a Distorted Sinusoidal Signal Using Analog Circuit

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Abstract—This paper proposes a method for zero-crossing approximation of a band-limited sinusoidal signal embedded by a white Gaussian noise-like distortion. It consists of passive low-pass filter and dynamic-hysteresis comparator circuits. Simplicity and wide dynamic range are the main goal of the proposed approach. Theoretical calculations were formulated to select proper circuit components values. Simulation and experimental results are then presented to show circuit performance and characteristics. The method approximates zero crossing within a certain boundary of small phase-shifts around the crossing signal. It utilized over a wide range of input amplitude and frequency variations.

I. INTRODUCTION

One way to reduce power loss in a power converter is to utilize a zero-current switching (ZCS). The method involves toggling a power switch when current is not flowing through it. For an AC/AC converter with a resonant circuit given in [1] and [2], ZCS is performed during zero-current crossing (ZCC). Therefore ZCC information from the measured resonant current is needed. In practice, distortions are usually present in a measured signal, which typically has a behavior similar to white Gaussian noise (WGN). This makes zero-crossing detection (ZCD) a challenge [3] [4] [5].

Currently available ZCD methods suffer from at least one disadvantage that is summarized in [3], [6] and [7]. Some notable drawbacks are:

- 1) Added phase-shift due to filtering that displaces zero-crossing positions of original signal;
- 2) Decreased performance because of sensitivity to input and filter parameters variations;
- 3) Need of high-speed processor to compensate slow dynamic response that can increase system complexity and cost.

To address the issues, a different approach to detect zero-crossing is given in this paper. Input harmonics are partially filtered by a passive R-C low-pass filter (LPF) with a high cut-off frequency to minimize phase-shift. Dynamic-hysteresis comparator (DHC) circuit is then utilized to remove multiple switchings around input transition level. The method is applicable to a band-limited sinusoidal signal added with a limited

crest factor WGN distortion. The proposed method emphasized on circuit simplicity and wide input signal dynamic range.

This paper is organized as follows. Explanation on zero-crossing approximation (ZCA) method is described in Section II. Section III deals with circuit components selections for LPF and DHC. Simulation results are analyzed and given in Section IV. Results of experimental validation are shown in Section V. Finally, conclusion of the paper is given in the last section.

II. ZERO-CROSSING APPROXIMATION PRINCIPLE

Schematic of ZCA circuit is shown in Fig. 1. It consists of passive LPF connected to DHC. Output side of DHC can optionally be forwarded to an edge-triggered circuit (ETC). The ETC creates pulses during transition from low to high or vice versa [5].

Fig. 1. A complete ZCA schematic.

ZCA mechanism during one period of input, as well as voltage informations are described in Fig. 2. In Fig. 2a, a LPF with resistance R_f and capacitance C_f is used to reduce root-mean-square (RMS) value of input noise. Its cut-off frequency is selected in a way that output phase-shift is limited under a certain range. Therefore, frequency and amplitude ranges of input signal fundamental component must also be limited. In Fig. 2b, DHC removes multiple switchings around DHC offset voltage V_{off} , which in this case equals zero. Lastly, edge-triggered circuit transforms rising and falling edges of $V_{co}(t)$ to short pulses $V_{out}(t)$ as shown in Fig. 2c.

A. Dynamic Hysteresis Comparator Circuit

The main component of the proposed ZCA is a DHC, and it is used to eliminate multiple switchings during crossing. A simple DHC circuit for ZCA is explained in [3]. It utilizes a

Fig. 2. Basic principle of zero-crossing detection. The offset of $V_s(t)$ and V_{off} equal zero.

parallel R-C circuit on the positive feedback of an operational amplifier (op-amp) to shape its reference voltage. Unfortunately, electric components selection is not explained in detail in the paper. Therefore, an alternative op-amp-based circuit with a dynamic hysteresis characteristic is proposed. The schematic is given in Fig. 3.

Fig. 3. An op-amp-based dynamic hysteresis comparator circuit.

The dynamic hysteresis is achieved by combining the comparator U_1 with a differentiator consisting of R_d and C_d . The hysteresis level is shaped by exponential decay voltage $V+(t)$ of the R-C circuit. V_{off} is provided to give either a positive or a negative offset to the hysteresis level. It should be noted that the comparator is in a dual-supply configuration with V_{CC} and V_{EE} as positive and negative supply voltages respectively. Fig. 4 illustrates circuit's voltages behavior where a sine wave with constant amplitude V_a and constant period T_{in} is used on the input side. It is assumed that V_{off} has a positive value, $V_{co}(t)$ range is from 0 to V_{CC} , and $V+(t)$ level can be accepted by the comparator. In this case, zero-crossing toggle of $V_{co}(t)$ under a sinusoidal input is achieved if V_{off} is zero and V_{tot} equals to V_{CC} .

It can be seen that the toggling of $V_{co}(t)$ occurs during a transition either from $V_{in}(t) < V+(t)$ to $V_{in}(t) > V+(t)$ or vice versa. R-C time constant of the differentiator has to be much smaller than a half period of input frequency $V_{in}(t)$, so the comparator is triggered when the input crosses V_{off} . The exponential decay of $V+(t)$ is governed through a following equation,

$$V+(t) = V_{CC} \left[\exp\left(-\frac{t}{R_d C_d}\right) \right] + V_{off}. \quad (1)$$

Fig. 4. DHC signal waveforms. $V+(t)$ indicates a feedback voltage to the positive input of the op-amp, while V_{tot} is its maximum voltage. $V_{tot} - V_{off} = V_{CC}$.

Since in practice the input range is usually limited to a supply voltage range, a clipping or biasing circuit can be used on the negative input side as a safety measure [3][5]. If the offset voltage is needed, $V+(t)$ must be kept below input voltage limit. It can be done by reducing the level of output HIGH state with a comparator that has separate input and output supplies, such as LT1719 [8].

For a band limited sinusoidal $V_{in}(t)$ embedded with a WGN, DHC removes multiple switchings at the zero-crossing under certain conditions, compared to a comparator without hysteresis [5]. The conditions is explained in the next section. In comparison with a Schmitt trigger [5], the DHC can lead to an advanced crossing output since the noise boundary of $V_{in}(t)$ touches $V+(t)$ first, as illustrated in Fig. 2b. It must be mentioned that the DHC will oscillate indefinitely if $V_{in}(t)$ contains only noise voltage with an average equals to V_{off} .

III. CIRCUIT COMPONENTS CONSIDERATIONS

Some assumptions for $V_s(t)$ in Fig. 1 are made to aid component selections calculations, which are:

- 1) It is assumed that input signal $V_s(t) = V_f(t) + V_n(t)$, where $V_f(t)$ and $V_n(t)$ are input fundamental and noise voltages correspondingly. Both parameters are independent to each other.
- 2) The input fundamental is a sinusoidal signal that has constant amplitude V_a and constant frequency f_{in} as well as a zero offset.
- 3) The noise voltage used for modeling is assumed to be a discrete-time WGN with σ_n standard deviation and a known constant sample time, where $V_a > \pm 3\sigma_n$ ($\pm 3\sigma$ corresponds to 99.7% contribution [9]).

A. Passive Low-Pass Filter Circuit

Two parameters are used to select passive components of LPF, which are phase-shift (ϕ) and RMS voltage ratio (ψ) between output and input sides. For a WGN case, its standard deviation of voltage amplitude equals RMS value [9][10]. The

two parameters are calculated by separating fundamental and noise components of the input. Illustrations are given in Fig. 5. In Fig. 5a, input to the LPF only contains fundamental voltage

Fig. 5. LPF parameters for component selections.

or $V_s(t) = V_f(t)$. Using a frequency domain approach, a phase-shift of the LPF output is given in [5] and can be calculated as,

$$\phi = -\tan^{-1}\left(\frac{f_{in}}{f_c}\right), \quad f_c = \frac{1}{2\pi R_f C_f}, \quad f_{in} < f_c, \quad (2)$$

where f_{in} and f_c are constant input fundamental and filter cut-off frequencies respectively. The value of f_c is chosen so the gain is as close as to 0 dB. On Fig. 5b, ψ is calculated using a stochastic process approach when $V_s(t) = V_n(t)$. Due to LPF, there is a reduction of standard deviation from σ_n in the input to σ_{io} in the output. The reduction ratio can be calculated from average power equation given in [10],

$$\sigma_{io} = \sqrt{\frac{T_s}{2\pi} \int_{-\pi/T_s}^{\pi/T_s} S_n(\omega) |H(\omega)|^2 d\omega}, \quad (3)$$

$$H(\omega) = \frac{1}{1 + j\omega R_f C_f}. \quad (4)$$

Parameter $S_n(\omega)$ is power spectral density (PSD) of input noise voltage, which equals to σ_n^2 in a discrete-time WGN case [11]. Parameter $H(\omega)$ is a transfer function of the LPF, while T_s is noise sample time. By solving the integration, further calculation leads to,

$$\psi = \frac{\sigma_{io}}{\sigma_n} = \sqrt{\frac{1}{2\beta} [\tan^{-1}(\beta) - \tan^{-1}(-\beta)]}, \quad (5)$$

$$\beta = \frac{\pi R_f C_f}{T_s}. \quad (6)$$

The task will be to choose R_f and C_f values where both ϕ and ψ are minimum according to a specific application.

B. Dynamic Hysteresis Comparator Circuit

By comparing Fig. 1 and 3, $V_{io}(t)$ is the same as $V_{in}(t)$. It should be noted that under distortion/noise, the R-C time constant of DHC's differentiator must not be too small to the order comparable to the distortion period. Very small time constant can cause multiple switchings of $V_{co}(t)$ when distorted $V_{in}(t)$ (due to remaining harmonics from LPF) crosses V_{off} voltage. The effect can be seen in Fig. 6 where V_{off} equals zero.

From the figure, t_{i1} marks a first transition between positive and negative input due to $V_{in}(t) < V_+(t)$. But because of a small R-C time constant, $V_{co}(t)$ is toggled prematurely at t_{i1}

Fig. 6. Multiple switchings problem during V_{off} equals zero. Rising edges of $V_{co}(t)$ are labeled by t_{i1} and t_{i2} .

where $V_{in}(t) > V_+(t)$. The number of multiple switchings increases as the R-C time constant gets smaller. If the DHC is used as a period calculator of a certain distorted periodic input, this behavior leads to a calculation error. Thus, a quantitative calculation is needed to select proper passive components for the differentiator.

Fig. 7 is given to aid the calculation process for zero V_{off} . Since the LPF only partially reduces noise in the signal source, remaining harmonics will appear at DHC input. The noise amplitude is assumed to oscillate between $\pm 3\sigma_{io}$ at maximum from its mean since it contributes 99.7% of all time according to Gaussian distribution [9]. The harmonics upper and lower boundaries are assumed to be smooth and marked by $V_{ub}(t)$ and $V_{lb}(t)$ respectively. The boundary voltages are also assumed that they can be approximated by a shifted input signal $V_{in}(t)$. The calculation is based on an ideal circuit.

Fig. 7. Boundary voltages illustration under assumed conditions.

Important transitions of boundary voltages are marked by t_1 to t_3 . Beginning of positive to negative transition due to $V_{lb}(t)$ is marked by t_1 . In the other hand, initial transition from negative to positive side due to $V_{ub}(t)$ is represented by t_3 . The expression of $V_{ps}(t)$ is given in (1) which is the positive input reference voltage, but with a time shift t_1 and zero offset. Equations of the input, $V_{ps}(t)$, as well as boundary voltages are given as follows,

$$V_{in}(t) = V_a \sin(\omega_{in} t), \quad \omega_{in} = 2\pi/T_{in}, \quad (7)$$

$$V_{ub}(t) = V_a \sin(\omega_{in} t) + 3\sigma_{io}, \quad (8)$$

$$V_{lb}(t) = V_a \sin(\omega_{in} t) - 3\sigma_{io}, \quad (9)$$

$$V_{ps}(t) = V_{CC} \left[\exp \left(- \frac{(t - t_1)}{R_d C_d} \right) \right], \quad (10)$$

$$t_1 = T_{in} \left[\frac{1}{2} - \frac{1}{2\pi} \arcsin \left(\frac{3\sigma_{fo}}{V_a} \right) \right], \quad (11)$$

$$t_3 = T_{in} \left[1 - \frac{1}{2\pi} \arcsin \left(\frac{3\sigma_{fo}}{V_a} \right) \right]. \quad (12)$$

The targets are to make $V_{ps}(t) > V_{ub}(t)$ at $t_1 < t < t_2$, as well as $V_{ps}(t)$ smaller than a certain limit value at t_3 . One method to solve the problem is to use a slope equation of $V_{ub}(t)$ at $T_{in}/2$ as a barrier where $V_{ps}(t)$ cannot pass when it decays during $t_1 < t < t_2$. The highest amplitude and the lowest frequency values of $V_{in}(t)$ is chosen to determine differentiator components R_d and C_d . The illustration is shown in Fig. 8, which is a magnified version of Fig. 7.

Fig. 8. DHC safety margin calculation.

Slope equation of $V_{ub}(t)$ at $T_{in}/2$ is labeled by $L_1(t)$. A and B are two random points on $V_{ps}(t)$ connected by an imaginary line parallel to $L_1(t)$. According to a mean value theorem explained in [12], there is at least one point between A and B curve that has a tangent line parallel to $L_1(t)$. This tangent line is denoted by $L_2(t)$. Through a derivative operation of (8) at $T_{in}/2$, $L_1(t)$ and $L_2(t)$ are described as follows,

$$L_1(t) = -V_a \omega_{in} t + 3\sigma_{fo} + V_a \pi, \quad (13)$$

$$L_2(t) = -V_a \omega_{in} t + V_a \omega_{in} \delta, \quad (14)$$

$$\delta = t_1 + R_d C_d \left[1 - \ln \left(\frac{V_a \omega_{in} R_d C_d}{V_{CC}} \right) \right] \quad (15)$$

Therefore, the requirement for the DHC to prevent multiple switchings, is to select R_d and C_d values in such a way that $L_2(t) > L_1(t)$ is always fulfilled under any amplitude and frequency ranges of $V_{in}(t)$,

$$L_2(t) > L_1(t), \quad (16)$$

$$V_a \omega_{in} \delta > 3\psi \sigma_n + V_a \pi. \quad (17)$$

Variable σ_{fo} is replaced by $\psi \sigma_n$. Another requirement to follow is,

$$V_{ps}(t_3) < V_{lim}, \quad (18)$$

where V_{lim} is a voltage limitation to be imposed at t_3 . This value must be very close to V_{off} , or zero in this case to prevent late toggling within one cycle of input fundamental signal.

IV. SIMULATION RESULTS

An example case is given to illustrate component selections and their results at a simulation level. The case has input and circuit characteristics given in Table I. The aim is to limit a phase-delay at the highest frequency, resulting a containment of zero-crossing output at a certain boundary around the actual crossing. PLECS software was used for the simulation. It uses Mersenne Twister algorithm as a white noise generator [13]. All electrical components involved are ideal and ETC is not used in this case, therefore $V_{co}(t) = V_{out}(t)$.

TABLE I
ZCA SIGNAL AND CIRCUIT CHARACTERISTICS

Parameters	Values
Noise RMS voltage (σ_n)	30 mV
Noise sample time (T_s)	1 ns
Fundamental amplitude (V_a) range	$10\sigma_n - 160\sigma_n$
Fundamental frequency (f_{in}) range	25 kHz - 50 kHz
Fundamental offset voltage	0 V
Filter capacitance (C_f)	220 pF
Comparator positive supply voltage (V_{CC})	5 V
Comparator negative supply voltage (V_{EE})	-5 V
Limit voltage (V_{lim})	1 nV

Requirements for the LPF is, at the maximum amplitude ($160\sigma_n$) and frequency (50 kHz), a desired phase-shift ϕ_d is chosen to be,

$$-\arcsin \left(\frac{3}{160} \psi \right) \leq \phi_d < 0, \quad (19)$$

where by looking at Fig. 7, the arcsine term is equal to the phase difference between (7) and (8), under the selected amplitude and frequency. Plots of ψ , ϕ and ϕ_d with respect to R_f is given in Fig. 9. From the bottom sub-figure, the crossing point between ϕ and ϕ_d is a desired resistance, which is close to 55 Ω . For a DHC case, (17) must be fulfilled at the lowest

Fig. 9. Plots of ψ , ϕ and ϕ_d using a constant value of $C_f = 220$ pF. Top and bottom plots have the same x-axis scale and label.

operational amplitude and frequency, which are $10\sigma_n$ and 25 kHz correspondingly. Calculation results are summarized in Table II and III. Simulation results are given in Fig. 10-12. The ψ values from Table II and simulation data are similar.

Fig. 11 and 12 contain one fundamental cycle comparison between filter output $V_{fo}(t)$ and fundamental input $V_f(t)$ voltages with a relation to $V_{out}(t)$. Right-half of Fig. 11 and 12 are zoomed versions of their left-half around zero-crossing. Time difference between $V_f(t)$ and $V_{out}(t)$ is marked in the bottom-right plot by a circle in each corresponding figure.

TABLE II
CALCULATION RESULTS FOR LPF ($V_a = 160\sigma_n$, $f_{in} = 50$ kHz)

Parameters	Values
R_f	51Ω
C_f	220 pF
f_c	14.185 MHz
ϕ	$-3.525 \cdot 10^{-3} \text{ rad}$
ψ	$2.092 \cdot 10^{-1}$

TABLE III
CALCULATION RESULTS FOR DHC ($V_a = 10\sigma_n$, $f_{in} = 25$ kHz)

Parameters	Values
R_d	47Ω
C_d	4.7 nF
$V_a \omega_{in} \delta$	$9.94 \cdot 10^{-1}$
$3\psi\sigma_n + V_a\pi$	$9.613 \cdot 10^{-1}$
$V_{ps}(t_3)$	$7.216 \cdot 10^{-20} \text{ V}$
V_{off}	0 V

Fig. 10. Plots of $V_s(t) = V_n$ before and after LPF. From the data, RMS voltage or standard deviation is $30.022 \cdot 10^{-3}$ before LPF, and becomes $6.241 \cdot 10^{-3}$ after filtering. Therefore, ψ from the simulation is $2.079 \cdot 10^{-1}$. Top and bottom plots have the same x-axis scale and label.

On the bottom-right of Fig. 11, there is an early toggle of $V_{out}(t)$. It is about 93.776 ns earlier ($1.473 \cdot 10^{-2} \text{ rad}$) than $V_f(t)$ crossing. Negative phase-shift effect due to filtering is not apparent due to remaining noise fluctuation. Meanwhile, the phase-shift effect is clear in Fig. 12 due to higher frequency of the input. It shifts $V_{out}(t)$ 15 ns later ($-4.712 \cdot 10^{-3} \text{ rad}$) after the fundamental signal crossing.

V. EXPERIMENTAL RESULTS

A circuit was built and tested to verify the proposed ZCA concept. Experimental verification focuses on analyzing

Fig. 11. Simulation results comparison for $V_a = 10\sigma_n$, $f_{in} = 25$ kHz. Parameter $V_{out}(t)$ is scaled to 0.3 V for clarity. Time difference marked in bottom-right plot by a circle is 93.776 ns.

Fig. 12. Simulation results comparison for $V_a = 160\sigma_n$, $f_{in} = 50$ kHz. Time difference marked in bottom-right plot by a circle is 15 ns.

DHC performance, thus ETC was not included in the circuit. Therefore in this case $V_{co}(t) = V_{out}(t)$. Circuit appearance with detailed components description is given in Fig. 13. Tektronix AWG2005 was chosen to generate various noise-embedded input sinusoidal signals similar to the simulation case. The noise crest-factor was set to 3, which corresponds to an area of $\pm 3\sigma_n$ of Gaussian distribution. Input noise RMS-voltage or σ_n was set to $30 \text{ mV}_{\text{RMS}}$.

Experimental data were taken by Tektronix TPS 2014B oscilloscope and their plots were reproduced by MATLAB for a better presentation. The voltage plots of input $V_s(t)$, filter output $V_{fo}(t)$, DHC output $V_{out}(t)$ and reference $V_{ps}(t)$ for different input characteristics are presented in Fig. 14-16. Fig. 14 correlates to a case with an amplitude of $10\sigma_n$ and frequency of 25 kHz. It can be seen that there are multiple switchings during zero-crossing transitions. This is

Fig. 13. Printed circuit board (PCB) and components description of ZCA circuit without ETC. Component symbols are based on schematics given previously in Fig. 1 and 3.

due to small R-C time constant of the differentiator circuit explained in Section II. This result is different than in the simulation because there was an exclusion of component's tolerance values in the calculation. Therefore, it is advisable to use either a bigger safety margin or high precision components for both LPF and differentiator circuits. Temperature variations and components' aging must also be taken into consideration. Multiple switchings during input transitions cease to exist when the input V_a equals $20\sigma_n$ as shown in Fig. 15. Fig. 16 illustrates voltage behaviors at the highest amplitude and frequency. Since the V_a is much bigger than $\pm 3\sigma_n$, the detection works well in this case. Unfortunately, phase-shift effect was not measured in practical case due to limited time.

Fig. 14. Experimental results for $V_a = 10\sigma_n$, $f_{in} = 25$ kHz.

Fig. 15. Experimental results for $V_a = 20\sigma_n$, $f_{in} = 25$ kHz.

Fig. 16. Experimental results for $V_a = 160\sigma_n$, $f_{in} = 50$ kHz.

VI. CONCLUSION

A simple zero-crossing approximation circuit has been proposed and analyzed in this paper. It consists of passive low-pass filter, dynamic-hysteresis comparator and optional edge-triggered circuits. The circuit can be used to apply a zero-current switching mechanism in a power converter. Component selections based on theoretical analysis were explained and verified by a computer simulation. At the simulation level, the circuit can detect zero-crossing transitions at given amplitude and frequency ranges, within small phase-shifts boundary around actual crossing. The detection is more accurate when the input noise level is much lower than input fundamental amplitude. An actual circuit was manufactured and tested to show real performance of the approximation method. The circuit behavior follows the theoretical formulations. It must be noted that when the input contains only noise voltage which has the same average value than DHC offset voltage, the circuit will oscillate indefinitely.

The calculation of phase-shift, as well as a comparison of the proposed ZCA circuit with currently available ZCD methods will be analyzed in the future. Other possible usage of DHC will be studied and reported in future publications.

REFERENCES

- [1] F. P. Kusumah *et al.*, A Direct Three-Phase to Single-Phase AC/AC Converter for Contactless Electric Vehicle Charger, in *Proc. European Conference on Power Electronics and Applications*, Geneva, 2015, pp. 1-10.
- [2] Hao Leo Li *et al.*, A Direct AC-AC Converter for Inductive Power-Transfer Systems, *IEEE Transactions on Power Electronics*, vol. 27, pp. 661-668, Jun. 2011.
- [3] R. W. Wall, Simple Methods for Detecting Zero Crossing, in *Proc. 29th Annual Conference of the IEEE Industrial Electronics Society*, Roanoke, USA, Nov. 2003, pp. 2477-2481.
- [4] E. Irmak *et al.*, Design and Application of a Novel Zero-Crossing Detector Circuit, in *Proc. International Conference on Power Engineering, Energy and Electrical Drives*, Málaga, 2011, pp. 1-4.
- [5] P. Horowitz and W. Hill, *The Art of Electronics*, 3rd ed. New York, USA: Cambridge University Press, 2015.
- [6] R. Weidenbrüg and F. P. Dawson, New Synchronization Method for Thyristor Power Converters to Weak AC-Systems, *IEEE Transactions on Industrial Electronics*, vol. 40, pp. 505-511, Oct. 1993.
- [7] O. Vainio, S. J. Ovaska, Noise Reduction in Zero Crossing Detection by Predictive Digital Filtering, *IEEE Transactions on Industrial Electronics*, vol. 42, pp. 58-62, Feb. 1995.
- [8] Linear Technology. (2017, April 5). *LT1719 - 4.5ns Single/Dual Supply 3V/5V Comparator with Rail-to-Rail Output*[Online]. Available: <http://www.linear.com/product/LT1719>
- [9] C. D. Motchenbacher and J. A. Connelly, "Fundamental Noise Mechanisms," in *Low-Noise Electronic System Design*. New York, NY: John Wiley & Sons, Inc., 1993, pp. 5-37.
- [10] W. C. van Etten, *Introduction to Random Signals and Noise*. Chichester, UK: John Wiley & Sons Ltd, 2005.
- [11] R. M. Gray and L. D. Davisson, "Second-order theory," *An Introduction to Statistical Signal Processing*. Cambridge, UK: Cambridge University Press, 2004, pp. 275-362.
- [12] G. B. Thomas and R. L. Finney, "Applications of Derivatives," *Calculus and Analytic Geometry*, 9th ed. Addison-Wesley Publishing Company, 1996, pp. 189-274.
- [13] Plexim. (2017, April 5). *PLECS, The Simulation Platform for Power Electronic Systems (User Manual Version 4.0)*[Online]. Available: <http://www.plexim.com/files/plecsmanual.pdf>