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A 20-60GHz Digitally Controlled Composite Oscillator for 5G

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Abstract—This paper describes a frequency generator supporting over-an-octave tuning range for 5G receiver front-end. Generator is built by composition of smaller-range oscillators multiplexed to the common output that drives a downconversion mixer. Simulated in 28nm CMOS with full physical device models the composite oscillator exhibits a frequency tuning range from 21.5 to 60.7GHz (95.3%) dissipating less than 25.8mW from a 0.9V supply. As a result, it achieves -184dBc/Hz FOM_{TR}.

I. INTRODUCTION

Fifth generation (5G) communication networks, in the first phase, started their operation in traditional below-6GHz bands. To achieve up to 10Gb/s data-rate and up to 100Mb/s bandwidth, in the coming years 5G networks will utilize [1] mm-wave spectra in 24-28GHz, 37-48GHz ranges in United States and 24-27GHz range in Europe. Trial 5G network deployment already utilizes bands at 28GHz [2].

Communication hardware at these frequencies will be based on arrays of transceivers feeding phased array antennas [3] to provide steerable directivity (beamforming) and high gain. In this multi-IC scalable array scenario, need for TX/RX chips supporting various mm-wave bands will increase, calling for suitable architectures. One candidate for beamforming architecture is a superheterodyne type of transceiver [4],[5]. While having relatively low complexity, such arrangement requires local oscillator (LO) to support full frequency range of corresponding mm-wave front-end.

Development of full-range-chip for 5G, therefore, brings about a challenge of producing clock signal with over-an-octave frequency coverage. Widest tuning range in the mm-wave oscillators has been achieved with magnetically tuned elements [6] or switched inductors [7]. In contrast, at RFIC domain below 10GHz, common industrial-level approach is to utilize a set of narrow-tuning-range VCOs that provide low phase noise. This direction has yet received little attention at mm-wave frequencies.

In the paper we describe design of a frequency source with multiplexed oscillators to support over-an-octave tuning range. Proposed 20GHz-60GHz generator attempts to aggregate present and future bands of 5G NR specification.

This paper is organized as follows. System trade-offs of wide-tuning range LC-tank oscillator are discussed in Section II, while Section III covers details of multiplexing and

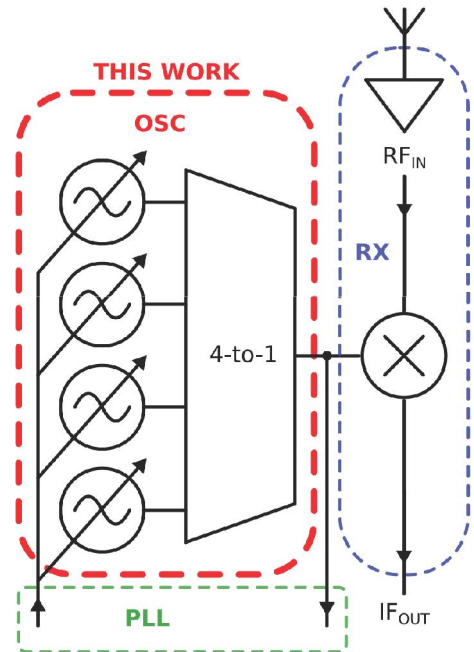


Fig. 1: Scope of the paper: frequency source for 5G

buffering chains. In Section IV we summarize schematic-level simulated performance of the complete LO chain.

II. COMPOSITE MM-WAVE OSCILLATOR

A. Motivation

For a hypothetical implementation of wide-tuning range LC-type oscillator as a single coil with a switchable capacitors bank, one can derive the output frequency expression:

$$F_O(\Delta C) = \frac{1}{2\pi\sqrt{L(C_0 + \Delta C)}}, \quad (1)$$

where $\Delta C \in [0; \Delta C_{MAX}]$ is the difference between capacitance states, switchable by external means and C_0 - capacitance in LC-tank, that can not be reduced (total C_{LOW} -state of all varactors, lumped parasitics of all wires, etc.)

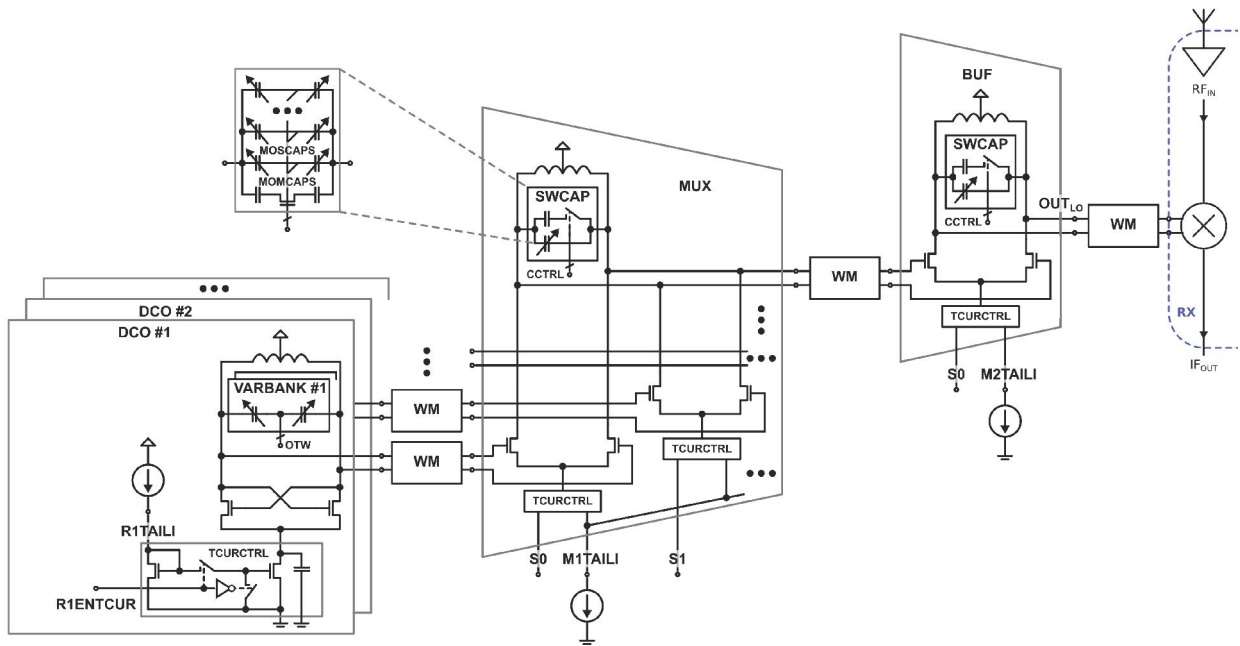


Fig. 2: Block diagram of the composite oscillator for 5G.

On the one hand, for a ballpark mm-wave inductor value of $L = 150\text{pH}$ in (1) one yields for $F_{O\ MIN} = 20\text{GHz}$ and $F_{O\ MAX} = 60.7\text{GHz}$:

$$\begin{aligned} F_{O\ MAX} &\Rightarrow C_0 \approx 50\ \text{fF}, \\ F_{O\ MIN} &\Rightarrow C_0 + \Delta C_{MAX} \approx 0.5\ \text{pF}. \end{aligned} \quad (2)$$

Unfortunately, one order of magnitude for capacitance range cannot be produced by varactors bank, since parasitic capacitance will then amount to a greater and unswitchable part of the total capacitance. Moreover, quality factor of varactor degrades quickly with frequency [8],[9] reducing LC-tank tuning range.

On the other hand, from digital control perspective, if the bus of width M governs the binary weighted varactors in capacitors bank and optimistic tuning range of individual varactor is $C_{HIGH}/C_{LOW} \approx 2$ then:

$$\frac{C_{HIGH}}{C_{LOW}} = 1 + \frac{\Delta C_{LSB}}{C_{LOW}} = 1 + \frac{(2^M - 1)\Delta C_{LSB}}{C_0} \approx 2, \quad (3)$$

ΔC_{LSB} being the difference between capacitance states enabled with the least significant bit of control bus. To reach $F_{O\ MIN}$ from (2) with M bits one must also require:

$$(2^{M-1} - 1)\Delta C_{LSB} = \Delta C_{MAX} \approx 450\ \text{fF}. \quad (4)$$

Conclusion is that for the desired tuning range equations (3) and (4) impose conflicting limitations on ΔC_{LSB} , which cannot be met with any number of bits M controlling the varactors bank. The described engineering considerations have not accounted for signal routing, tank losses, area penalty, which render a single-coil 20-60GHz range oscillator impossible.

B. Implementation

To resolve conflicting requirement discussed above and based on the previous expertise of the research group [10], we propose mm-wave frequency source (Fig. 2) comprised of *four* conventional tail current biased digitally controlled LC oscillators (LC-type DCO). Recently, two mm-wave oscillators has been demonstrated on the same die [11] proving feasibility of the taken approach.

With 4 oscillators, the desired 40GHz tuning range is broken into four bands (DCO1: 21.5–30.1GHz, DCO2: 28.9–39.1GHz, DCO3: 37.6–50.1GHz and DCO4: 48.7–60.7GHz) with the main advantage being that tuning elements for each band can now be made physically realizable and suitable for operation within PLL.

To ensure wide overall tuning range in presence of process variations a 6-7% overlap is secured for adjacent bands.

Unused DCOs are shut-down via TCURCTRL block functionality (signal R1ENTCUR in Fig. 2) to avoid frequency pulling and to decrease power consumption.

III. 4-TO-1 MM-WAVE MULTIPLEXER AND BUFFER

Wide frequency range multiplexing and buffering is another challenge that stems from combining several oscillators. For instance, in [12] a chain of current-mode logic buffers loaded with 4 single spiral transformers and an active negative feedback is proposed to achieve -3dB bandwidth of 73.6GHz. The cited example does not have multiplexer functionality and can not be adopted here due to area penalty of multiple inductors.

In our work, a cascade of two tunable blocks - multiplexer and buffer - is proposed to achieve required -3dB bandwidth.

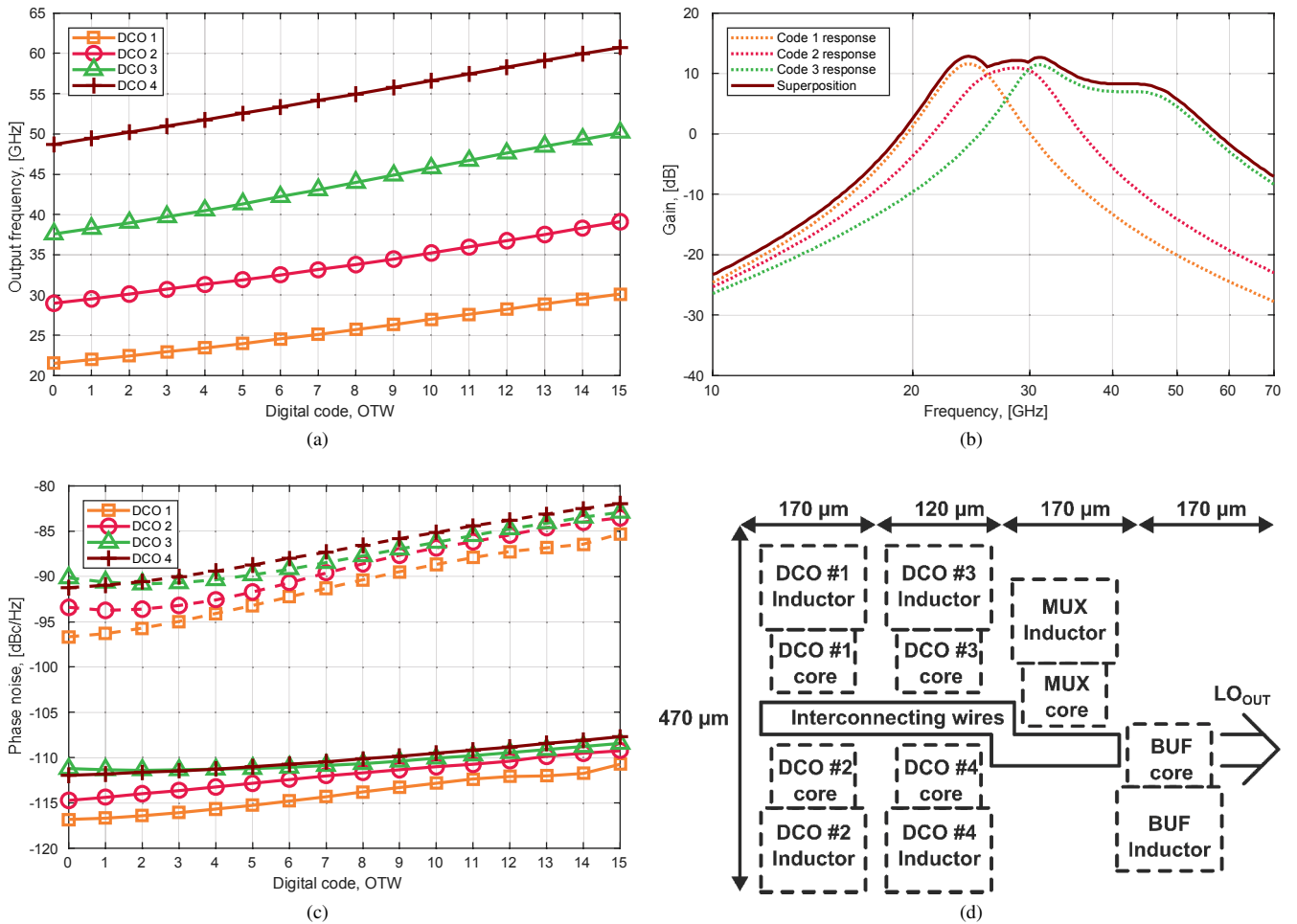


Fig. 3: (a) Tuning range versus control code for individual DCOs; (b) frequency response of the combined multiplexer-buffer chain for some illustrative codes; (c) phase noise at 1MHz (dashed line) and 10MHz (solid line) offsets versus control code for individual DCOs and (d) tentative floorplan of the composite oscillator

A. Multiplexing

In regards to multiplexing more than two inputs, different strategies can be applied. For the use-case in Fig. 1, one approach is to design 2-to-1 multiplexer and reuse it 3 times in a tree-like structure. Another strategy is to implement full 4-to-1 multiplexer. In mm-wave range, however, coils are added to resonate parasitic capacitance associated with the common nodes, making the tree-like structure coil-hungry and impractical.

4-to-1 tunable multiplexer designed in this work (MUX in Fig. 2) encompasses four differential pairs with inductive load. To bring inductance to the range of pico-Henrys and further save area, loading inductors are merged into a single central-tapped inductor. For the frequency response tuning, a capacitors bank is connected in parallel with the inductor. Two different configurations are employed: MOM capacitors and MOS varactors in a differential, switchable from the bus arrangement.

B. Buffering

For the full chain bandwidth enhancement, and simultaneously for multiplexer output swing amplification, a tunable buffer is applied at the output of 4-to-1 multiplexer. The buffer (BUF in Fig. 2) is designed as a copy of the aforesaid multiplexer with the capacitors bank values shifted towards bigger values, to enable two distinct resonances in the multiplexer-buffer chain.

IV. CIRCUIT SIMULATION RESULTS

Entire LO chain has been assembled, loaded with a double-balanced mixer and simulated in 28nm CMOS with full physical device models. To account for routing, a pessimistic π -section model of interconnecting wires (WM in Fig. 2) is inserted in-between the blocks with $R=20\Omega$, $L=10\text{pH}$ and $C=20\text{fF}$.

For all the control codes Fig. 3a combines tuning ranges of the individual DCOs and Fig. 3c shows phase noise plots at 1MHz and 10MHz offset frequencies.

TABLE I: Performance summary and comparison with the state-of-the-art.

	This work	JSSC'13 [6]	IMS'14 [13]	JSSC'15 [7]	MTT'15 [14]
Frequency range widening mechanism	Oscillators bank	Switched-triple shielded transformer	Transformer-coupled resonators	Stacked switched inductors	Tunable transmission lines
CMOS process	28 nm	65 nm	45 nm	65 nm	65 nm
Area	0.017 mm ²	0.03 mm ²	0.021 mm ²	0.55 mm ²	0.0075 mm ²
Supply voltage	0.9 V	1.2 V	1.0 V	1.5 V	1.0 V
Power dissipation	23.8 mW (21.5 GHz) 25.8 mW (60.7 GHz)	8.4 mW (57.5 GHz) 10.8 mW (90.1 GHz)	8 mW (21 GHz) 16 mW (54.6 GHz)	30 mW (85 GHz) 45 mW (127 GHz)	21.5 mW (70.4 GHz)
Frequency range	21.5 ... 60.7 GHz	57.5 ... 90.1 GHz	21 ... 54.6 GHz	85 ... 127 GHz	55.1 ... 70.4 GHz
Tuning range	95.3 %	44 %	88.4 %	38.8 %	24.4 %
Results type	Schematic-level simulated	Measured	Measured	Measured	Measured

To support fair comparison between individual DCOs and frequency source as a whole, we adopted Figure-of-Merit [15] that includes both tuning range and power consumption

$$FOM_{TR} = PN_{10MHz} - 20\log_{10}\left(\frac{F_{OUT}}{10MHz} \cdot \frac{TR_F}{10}\right) + 10\log_{10}\left(\frac{P_{DISS}}{1mW}\right), \quad (5)$$

yielding $FOM_{TR} \approx -189\text{dBc/Hz}$ with $F_{OUT} = 60.7\text{GHz}$, $P_{DISS} = 25.8\text{mW}$, $TR_F = 95.3\%$ and $PN_{10MHz} = -108\text{dBc/Hz}$.

Tunable frequency response of multiplexing and buffering chain is given in Fig. 3b. Finally, Fig. 3d demonstrates tentative floorplan (630 μm x 470 μm) of the LO chain. Simulation results of the LO chain are compared in the Table I with the state of the art.

V. CONCLUSION

An idea of composite DCOs covering over-an-octave tuning range has been explored. The main functional blocks of the composite DCO were the oscillators bank, the tunable 4-to-1 multiplexer and the tunable buffer. It was simulated that composite DCO achieves a frequency tuning range of 21.5 to 60.7GHz (95.3%) dissipating less than 25.8mW from a 0.9V supply.

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