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*Published in:*

2018 IEEE International Symposium on Circuits and Systems, ISCAS 2018 - Proceedings

*DOI:*

[10.1109/ISCAS.2018.8350977](https://doi.org/10.1109/ISCAS.2018.8350977)

Published: 26/04/2018

*Document Version*

Peer reviewed version

*Please cite the original version:*

Lemberg, J., Kosunen, M., Nieminen, T., Roverato, E., Martelius, M., Stadius, K., ... Valkama, M. (2018). Design and Implementation of a Wideband Digital Interpolating Phase Modulator RF Front-End. In 2018 IEEE International Symposium on Circuits and Systems, ISCAS 2018 - Proceedings (Vol. 2018-May). [8350977] (IEEE International Symposium on Circuits and Systems proceedings). Institute of Electrical and Electronics Engineers. <https://doi.org/10.1109/ISCAS.2018.8350977>

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# Design and Implementation of a Wideband Digital Interpolating Phase Modulator RF Front-End

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**Abstract**—This paper describes implementation details of a digital-intensive phase modulator architecture that does not require a frequency synthesizer to cover a wide carrier frequency range. The phase modulator operation is based on toggling the output accurately during the sample period to generate the phase-modulated signal. The toggling instants within the sample period are calculated by DSP solvers that utilize linear interpolation. The interpolation effectively multiplies the phase signal sample rate by the modulator phase resolution, which enables wider signal bandwidth and a completely digital method of defining the transmitter carrier frequency. The phase modulator concept is verified by implementing it as a part of an outphasing transmitter in 28 nm CMOS. With a constant sample rate of 1.5 GHz and without any predistortion, the transmitter achieves better than -28 dBc ACLR with 100 MHz aggregated LTE downlink signal between 0.8–2.0 GHz carrier frequency.

## I. INTRODUCTION

The well-known software defined radio paradigm calls for digital transmitters with highly reconfigurable signal bandwidth and carrier frequency. One digital-intensive transmitter architecture is outphasing, as it can operate by solely utilizing phase-modulated rail-to-rail signals. Thus, the phase-modulated signals can be generated with digital-intensive circuitry and further amplified with highly efficient switched-mode power amplifiers.

In order to improve the outphasing transmitter linearity, we have proposed the concept of digital interpolating phase modulator (DIPM) in [1]. The DIPM linearly interpolates the phase signal at the transmitter sample rate in digital domain. This improves the transmitter linearity, as linear interpolation provides better sampling image attenuation than sample and hold, which is utilized in conventional digital phase modulators [2]–[5]. In [6], we have reported measurement results of a multilevel outphasing transmitter utilizing the DIPM. The implementation was capable of up to 400 MHz instantaneous bandwidth with the ability to generate the carrier between 0.35–2.6 GHz with a constant input clock frequency.

In this paper, we present the details regarding the design and implementation of a digital-intensive outphasing transmitter that utilizes DIPMs to achieve wide signal bandwidth. Furthermore, the technique enables digital carrier generation that provides a completely digital way of defining the carrier frequency, independent of the input clock frequency of

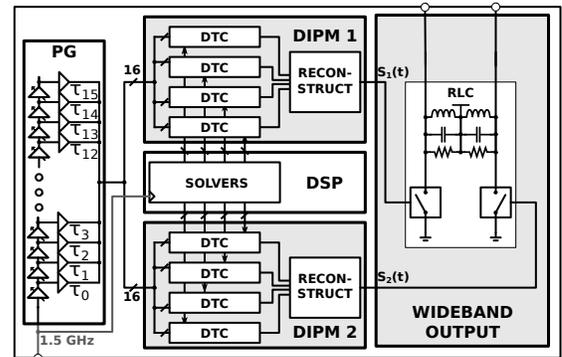


Fig. 1. Outphasing transmitter block diagram with focus on the RF front-end.

the transmitter. The new measurements shown in this paper demonstrate that the outphasing transmitter prototype is capable of transmitting 100 MHz aggregated LTE signal with -28 dBc adjacent channel leakage ratio (ACLR) between 0.8–2.0 GHz carrier frequency by utilizing constant 1.5 GHz sample rate. Thus, the DIPMs enable the transmitter to cover a wide carrier frequency range without a frequency synthesizer.

Section II discusses the implemented outphasing transmitter architecture, whereas Section III explains the concept of phase interpolation. The implementation details of the phase modulator RF front-end are described in Section IV, measurement results are shown in Section V and conclusions in Section VI.

## II. OUTPHASING TRANSMITTER ARCHITECTURE

The developed digital interpolating phase modulator (DIPM) has been implemented as a part of an outphasing transmitter. In outphasing, the amplitude- and phase modulated signal  $V(t)$  is formed by combining two constant-amplitude phase-modulated signals as

$$V(t) = S_1(t) + S_2(t) \quad (1)$$

$$S_{1,2}(t) = \cos(\omega_c t + \Phi_{1,2}(t)), \quad (2)$$

where  $\omega_c$  is the angular carrier frequency. Phase modulation is performed by  $\Phi_{1,2}(t)$ , which contains the polar angular component  $\phi(t)$  and the outphasing angle  $\theta(t)$  that defines amplitude modulation as

$$\Phi_1(t) = \phi(t) + \theta(t), \quad \phi(t) \in [0, 2\pi[ \quad (3)$$

$$\Phi_2(t) = \phi(t) - \theta(t) \quad (4)$$

$$\theta(t) = \arccos(r(t)), \quad \theta(t) \in [0, \frac{\pi}{2}], \quad (5)$$

where  $r(t)$  is the normalized signal envelope.

The block diagram of the outphasing transmitter, with focus on the blocks presented in this paper, is shown in Fig. 1. The DIPMs generate the phase-modulated signals  $S_1(t)$  and  $S_2(t)$ . Each phase modulator utilizes 16 evenly distributed coarse phases, which are generated with a phase generator (PG) from the 1.5 GHz input clock. The PG consists of a tapped delay line with digitally tunable delay. The phase-modulated signals generated with the DIPMs are fed to a wideband output stage that contains a wideband RLC resonator with center frequency at 1 GHz.

### III. PHASE INTERPOLATION

This section explains how sample-and-hold in the phase modulator limits the outphasing transmitter linearity, and describes how linear interpolation is utilized in the DIPM architecture to solve the problem.

#### A. Linearity degradation due to Sample-and-Hold

In conventional digital-intensive phase modulators [2]–[5] the local oscillator (LO) signal is simply delayed as a function of the phase signal. Thus, the modulated square-wave LO waveform with 50% duty cycle can be presented in its Fourier series form as

$$S_{sq}(t) = \sum_{k=1}^{\infty} \frac{4}{n\pi} \cos(n(\omega_c t + \Phi_{sh}(t))), \quad n = 2k - 1, \quad (6)$$

where  $\Phi_{sh}(t)$  includes the sample-and-hold of digital controls. By investigating the  $n$ th harmonic of  $S_{sq}(t)$ , it can be observed that in addition to  $\omega_c t$ , also  $\Phi_{sh}(t)$  is multiplied by  $n$  as

$$S_{harm}(t, n) = \frac{4}{n\pi} \cos(n\omega_c t + n\Phi_{sh}(t)). \quad (7)$$

As the outphasing angle is defined between  $[0, \frac{\pi}{2}]$  to represent normalized signal magnitude between  $[0, 1]$ , multiplying it by  $n$  corrupts the amplitude modulation at LO harmonics when the signals  $S_{1,2}$  are combined. The individual harmonics of the RF signal  $V_{harm}(t, n) = S_{1,harm}(t, n) + S_{2,harm}(t, n)$  are shown in Fig 2, demonstrating how the sampling images of  $\Phi_{sh}(t)$  that intermodulate with carrier harmonics  $n$  are not recombined correctly. The sampling images fall on the signal band and limit the outphasing transmitter linearity.

Thus, the problem can either be solved by filtering the sampling images or the LO harmonics. As the square-wave LO is inherent in digital circuits, suppressing the sampling images is more feasible. Conventionally, sample rate is increased in order to push the images further, such that the *sinc* response of sample-and-hold attenuates the images sufficiently. However, modern CMOS limits the achievable sample rate of complex arithmetic operations to the order of few gigahertz, where state-of-the-art digital transmitters are already operated at. The linearity of a digital outphasing transmitter can therefore

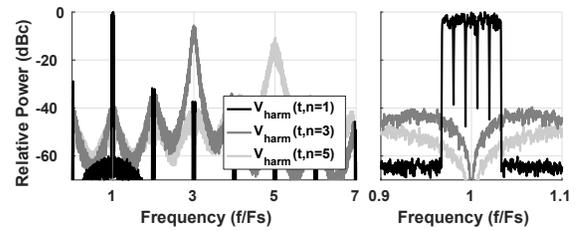


Fig. 2. System-level simulation depicting how sampling images in conventional digital outphasing transmitters limit transmitter linearity.

only be improved by replacing sample-and-hold with a more accurate signal estimation method.

#### B. Phase Interpolation Concept

One method that improves the image attenuation over the *sinc* response of sample-and-hold is to perform linear interpolation of the digital phase signal at the transmitter sample rate to achieve *sinc*<sup>2</sup> response. Performing linear phase interpolation with a conventional digital phase modulator is not possible, as the state of the phase-modulated rail-to-rail signal must be toggled at arbitrary times within the sample period.

The digital-intensive phase modulator architecture described in this paper solves the aforementioned problem, as it enables toggling the state of the output signal waveform arbitrarily up to four times within the sample period. The time-instants when the phase-modulated signal toggles are calculated by DSP solvers that utilize linear phase interpolation. The digital phase signal  $\rho[n]$  fed to the solvers is

$$\rho[n] = \alpha n + \Phi[n] \quad (8)$$

$$\alpha = 2\pi \frac{f_c}{F_s}, \quad (9)$$

where  $\alpha$  is a constant phase increment that defines the carrier frequency as a function of sample rate. In short, the solvers calculate the instants during the sample period where  $\rho[n] - \rho[n - 1]$  crosses integer  $\pi$  values, indicating a 180 deg phase shift when the DIPM RF front-end output should toggle. Further details of locating the toggling instants with phase interpolation in digital domain, without increasing the transmitter sample rate, are explained in [1].

### IV. IMPLEMENTATION OF THE DIGITAL INTERPOLATING PHASE MODULATOR RF FRONT-END

Fig. 3 shows the block diagram of the DIPM RF front-end, which performs phase modulation by toggling the state of the rail-to-rail output waveform with delays as controlled by the DSP solvers at 1.5 GHz sample rate. The toggling signals are generated by four time-interleaved digital-to-time converters (DTC). Each DTC is capable of generating an accurately delayed pulse that toggles a rising-edge sensitive T-flipflop. Thus, each DTC pulse corresponds to changing the sign of the output waveform, and the continuous stream of combined DTC pulses reconstructs the phase-modulated signal. The phase modulator thus enables generating instantaneous frequencies

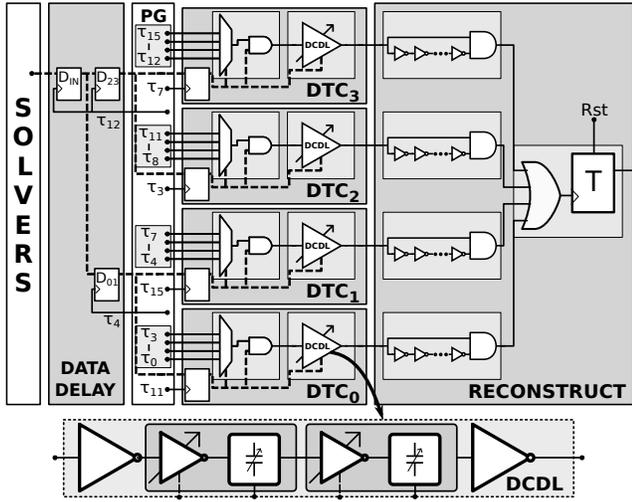


Fig. 3. Block diagram of the phase modulator RF front-end.

up to twice the phase modulator sample rate, while it does not limit the lowest instantaneous frequency that the phase modulator can produce. The DIPM thus completely reconstructs the phase-modulated RF signal, which removes the conventional dependency from the LO signal from the phase modulator RF front-end, and enables digital carrier generation.

The phase modulator targets 10-bit phase resolution at 1.5 GHz, corresponding to a delay range of 667 ps over 0.65 ps steps. Because of the large delay tuning range, a segmented approach was chosen. 16 coarse delays are generated with the phase generator to provide 4-bit resolution. The remaining 6-bit resolution is implemented with a digitally controlled delay line (DCDL) within each DTC.

#### A. Digital-to-Time Converter

Each digital-to-time converter in the phase modulator covers one fourth of the sample period and is controlled with 8-bit precision. In the input of each DTC, a coarse delay from the PG is first selected with a multiplexer (MUX). After the coarse delay has been selected, an enable signal controls with an AND gate to allow only desired pulses to propagate further. If the enable is set, the coarsely delayed signal with 50% duty cycle propagates to the digitally controlled delay line.

The DCDL delays the selected coarse delay with finer 6-bit resolution, corresponding to a delay range of 42 ps with 0.65 ps steps. The DCDL is designed in two cascaded stages to increase transition speed and thus decrease noise coupling in the loaded node. Each stage consists of an inverter with configurable driving strength to tackle process variations, and a varactor bank with tunable load capacitance for delay tuning.

#### B. Reconstruction Stage

The signal in the output of each DTC has 50% duty cycle, which is decreased in a pulse generator as it enters the reconstruction stage. The pulse generator is implemented with an AND gate and a cascade of odd number of inverters

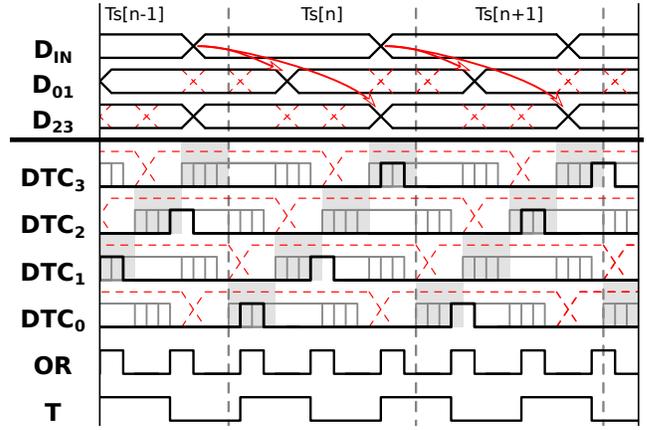


Fig. 4. Timing diagram of the phase modulator RF front-end, depicting reconstruction of a signal at  $3/2 F_s$ . For each DTC, the grey area shows the operating boundaries, the grey lines represent the selectable coarse phases and bolded black curves represent enabled transitions. The red dotted lines represent data signals and their clocking in the DTCs.

to produce approximately 100 ps pulse width. The pulses produced by the pulse generators can be combined in an OR gate without overlap, and used to toggle a T-flipflop sensitive to the rising edge. In order to ensure predictable behavior at power-on, reset functionality has been included in the T-flipflop.

#### C. Clocking Scheme

A timing diagram of the DIPM RF front-end is shown in Fig. 4, depicting the reconstruction of a tone at  $3/2 F_s$ . However, conventional digital phase modulators that simply delay the LO waveform would generate a modulated signal at  $3/2 F_s$  that suffers from duty cycle distortion and potentially generates unreproducible narrow pulses.

The figure also depicts how the data  $D_{IN}$  in the input of the modulator is shaped into delayed pulses in the DTCs that toggle the T-flipflop. Due to the fact that each DTC operates at a separate time slot sets further requirements on data synchronization, or otherwise the DTCs may generate incorrect pulses. For example, an erroneous pulse is generated if the DTC output is enabled while the MUX input is already high. Such an event has disastrous results for signal integrity, as the phase of the modulator output shifts 180 degrees. Thus, care must be taken to clock the DTC data while all MUX inputs are low to guarantee that the DTC operates correctly. A time window when MUX inputs are low exists only for  $T_s/4$  before the first rising edge to the MUX. As a consequence, each DTC must be clocked separately. The optimal clocking instants for each DTC are denoted in the figure with dashed red lines, allowing the DTC control signals to have sufficient time to settle before rising edges arrive to the MUX. In order to clock the DTCs accurately, the phase generator phases are also utilized as clocks. To provide sufficient timing margins for the data from the DSP solvers to each separately clocked DTC, an additional data delay block is first used to delay the

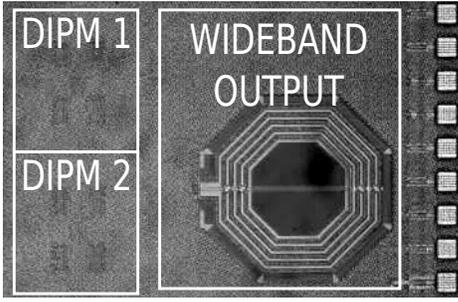


Fig. 5. The chip micrograph.

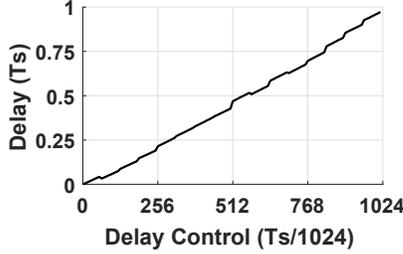


Fig. 6. The transfer curve based on on-chip linearity measurements.

input data separately to each DTC pair. The utilized clock signals in the implementation are shown in Fig. 3.

## V. MEASUREMENT RESULTS

The outphasing transmitter was fabricated in 28 nm FDSOI CMOS and directly wirebonded onto a measurement PCB. Fig. 5 shows the chip micrograph, where each DIPM RF front-end has an active area of  $0.18\text{mm}^2$  and consumes less than 16 mW. The phase signals are brought to the on-chip DSP solvers through an FPGA via a high-speed interface. The transmitter sample rate is fixed to 1.5 GHz while the carrier frequency is altered digitally by controlling the value of  $\alpha$ . The phase generator and the DCDL within each DTC have been calibrated with a combination of on-chip and off-chip measurements. The delay transfer curve produced by on-chip measurements is shown in Fig. 6. The phase generator delay tuning affects the whole chain, thus individual mismatches in the coarse delays cannot be corrected and remain after calibration. Furthermore, the chip does not contain predistortion hardware that is required to accurately predistort the solver outputs. As a consequence, the linearity of the DIPM RF front-end is degraded from the 10-bit target resolution.

The wideband capabilities of the outphasing transmitter are demonstrated with a 100 MHz aggregated non-contiguous LTE downlink signal in Fig 7(a) and 7(b). With the sample rate of 1.5 GHz and at the carrier frequency of 0.8 GHz the transmitter achieves -29 dBc ACLR. To the authors' knowledge, the digital transmitter in this work achieves the best reported ACLR with 100 MHz signal bandwidth at such a low carrier frequency. The frequency agility of the DIPM is further demonstrated with 100 MHz instantaneous bandwidth LTE signals at 1.8 GHz and 2.0 GHz carrier frequency

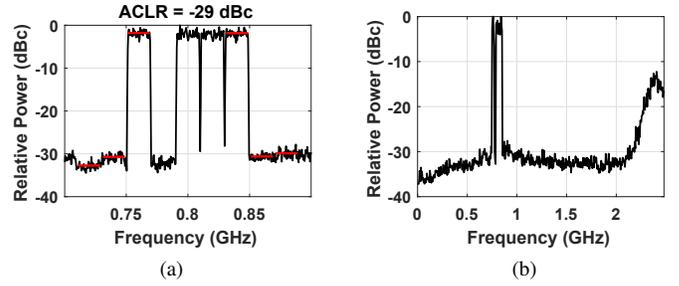


Fig. 7. (a) ACLR measurement using 1.5 GHz sample rate with a 100 MHz aggregated signal at 0.8 GHz carrier frequency, (b) wide-span spectrum.

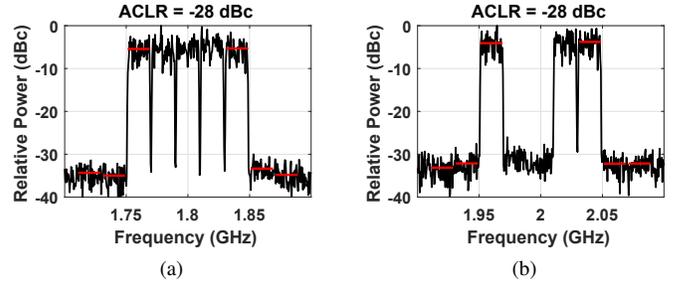


Fig. 8. ACLR measurements with 1.5 GHz sample rate using 100 MHz aggregated signals at (a) 1.8 GHz and (b) 2.0 GHz carrier frequency.

with constant 1.5 GHz sample rate. The resulting spectra are shown in Fig. 8(a) and in Fig. 8(b), demonstrating that phase interpolation enables digital control of carrier frequency without significant degradation in ACLR.

It must be further emphasized that the digital transmitter presented in this paper does not require that the carrier frequency is an integer multiple of the sample rate, as is required by conventional digital transmitters to constrain the sampling images in the spectrum. Thus, the phase interpolation performed by the DIPM successfully attenuates the sampling images, but the transmitter performance is limited by the transfer curve nonlinearity.

## VI. CONCLUSION

In this paper we presented a digital interpolating phase modulator (DIPM) RF front-end fabricated in 28 nm CMOS. The phase modulator was implemented as a part of an outphasing transmitter. The transmitter enables modulation with aggregated 100 MHz LTE signals with better than -28 dBc ACLR between 0.8–2.0 GHz carrier frequency by utilizing a constant 1.5 GHz sample rate, thus making external frequency synthesizers obsolete. The digital interpolating phase modulator was shown to enable wide carrier frequency range and signal bandwidth, making it a suitable building block for software defined radio transmitters.

## VII. ACKNOWLEDGMENT

This work is supported by Nokia, the Finnish Funding Agency for Technology and Innovation, and the Academy of Finland.

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