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A Configurable Sampling Rate Converter for All-Digital 4G Transmitters

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Abstract—This paper presents a digital interpolation chain for non-integer variable-ratio sampling rate conversion, targeted to 4G mobile applications. Such a system is needed in all-digital transmitters, where the sampling rate of the digital input to the RF front-end must be an integer fraction of the carrier frequency. A highly configurable architecture is proposed to cope with the flexibility needed in 4G applications. The system achieves excellent ACLR of 75 dB, EVM degradation of 0.05%, and RX-band noise below -160 dBc/Hz. Digital synthesis of the circuit in a 40nm low-power CMOS process results in a core area of only 0.073 mm². The estimated power consumption is between 6 and 29 mW, depending on channel bandwidth and transmission band.

I. INTRODUCTION

With the recent advance of deep sub-micron CMOS technologies, the design of RF circuits is being pushed more and more towards the digital domain. There, IC designers can exploit the growing availability of fast, cheap, and low-power digital logic, which compensates for the increasing difficulty of analog structures to offer adequate RF performance as transistor gate length and supply voltage decrease.

In the context of radio transmitters, starting from digital baseband modulators [1], [2], one step towards an “all-digital” solution is the Digital-to-RF Converter (DRFC) [3]–[7]. The DRFC suffers from two main problems: the quantization noise is only filtered by the RF matching circuitry, and the digital images are mainly attenuated by the *sinc* response of the D/A converter’s zero-order hold. However, increasing the oversampling ratio of the digital baseband signal can alleviate both effects to a level that can be handled in the RF domain, without need of complex analog bandpass filters.

In the DRFC, the sampling rate of the digital input should be an integer fraction of the LO frequency f_{LO} [4], [5]. When the DRFC is targeted to a specific radio standard, f_{LO} is usually specified to be changeable. Hence, a programmable fractional sampling rate converter has to be placed between baseband DSP processor and DRFC, as shown in Fig. 1. Such a sampling rate converter should also increase the oversampling ratio of the baseband signal as much as possible.

A programmable interpolation chain for a fully digital WiFi/WiMAX transmitter is described in [6], but only the 2.4–2.7 GHz frequency band is supported. Fractional interpolators

Fig. 1. Sampling rate converter as an interface between baseband processor and DRFC. Parameter D is integer.

are also used in the digital WCDMA transmitter presented in [7], although the interpolator details are not disclosed. This paper describes a programmable digital interpolation chain, targeted to all-digital 4G mobile phone transmitters. A new, highly configurable architecture is proposed, where the number and order of blocks is optimized for wide interpolation factor range, flexibility in the position of the digital images, as well as low power consumption. The interpolator has been specifically optimized for the LTE and LTE-A standards. Nevertheless, its use with other radio standards is not precluded, making it a suitable solution for multimode transmitters.

The paper is organized as follows. Section II discusses the system-level requirements for the interpolation chain. Section III describes the chosen system architecture and its implementation details. Some MATLAB simulation results are presented in Section IV. Section V reports the digital synthesis of the circuit. Finally, Section VI concludes the paper.

II. SYSTEM REQUIREMENTS

The requirements specified by the Long Term Evolution (LTE) cellular standard [8] bring a great deal of challenges to transmitter design [9], [10]. Flexibility and worldwide coverage are enabled by supporting a large number of operating bands between 0.7 and 3.8 GHz, as well as configurable channel bandwidth of 1.4, 3, 5, 10, 15, or 20 MHz. The emerging LTE-Advanced (LTE-A) further expands channel bandwidth configurability by introducing intra- and inter-band Carrier Aggregation (CA). Because a different base sampling frequency f_{in} corresponds to each channel bandwidth, the

Fig. 2. Functional block diagram of the proposed interpolation chain. The physical circuit includes some additional control logic, as well as I/O interfaces.

overall rate change factor required from the interpolation chain (which is directly proportional to f_{LO}/f_{in}) varies widely depending on the RF channel programming.

Both LTE and LTE-A support Frequency-Division Duplexing (FDD), where the duplex distance can be as small as 30 MHz in some operating bands. According to [7], [9], [10], the TX out-of-band noise that falls in the RX-band should be below -160 dBc/Hz, in order not to degrade the receiver sensitivity. If such requirement is not met, a Surface Acoustic Wave (SAW) filter is needed before the power amplifier, which is very undesirable in a multiband transmitter.

The -160 dBc/Hz RX-band noise requirement has important consequences on the interpolator design. The difference between the in-band power density level p_{Ch} and the noise floor in the RX-band n_f should fulfill

$$p_{Ch} - n_f > 160 - 10 \log_{10}(B_{Ch}) \quad [\text{dB}], \quad (1)$$

where B_{Ch} is the occupied channel bandwidth. Depending on the LTE / LTE-A bandwidth, a minimum power density difference ranging from 84 to 100 dB is revealed by (1). This determines the minimum digital word length to be used in the DSP blocks, since out-of-band noise in all-digital transmitters is dominated by quantization noise. Moreover, it calls for a flexible interpolation chain architecture. The location of the digital images on the frequency spectrum should be changeable, thus that it is always possible to move them away from the own RX-band, in any RF channel configuration. This is certainly more hardware and power efficient than designing a system with image attenuation higher than 100 dB.

III. SYSTEM DESIGN

The block diagram of the proposed interpolation chain is shown in Fig. 2. Each signal path (I and Q) consists of two Half-Band (HB) filters, one cubic Lagrange interpolator, and one Cascaded Integrator-Comb (CIC) interpolator. The programmable clock divider derives all the clocks used throughout the system from the LO signal, and it is shared among the I and Q paths. Input data samples are provided by an asynchronous time-interleaved interface (not shown in Fig. 2).

The final sampling rate of the output signal f_{out} cannot be arbitrarily large, for the circuit to be physically realizable. In this work, f_{out} is constrained within the range 699 - 1345 MHz by selecting:

- $f_{out} = f_{LO}$ for bands in the range 699 - 915 MHz;
- $f_{out} = f_{LO}/2$ for bands in the range 1427.9 - 2690 MHz;

- $f_{out} = f_{LO}/4$ for bands in the range 3400 - 3800 MHz.

A. General Guidelines

In small battery-powered applications such as mobile handsets, an important figure of merit is certainly power consumption. Therefore, the DSP front-end shown in Fig. 2 has been designed by keeping primarily in mind the low power budget. Small power consumption is obviously achieved in a digital design by minimizing the number of blocks in the circuit, the amount of hardware in each block, as well as the frequency at which each block is clocked.

B. Number of Bits

As stated in Section II, the dominant source of out-of-band noise in all-digital transmitters is quantization noise. If a signal with bandwidth B_s , sampled at rate F_s , is uniformly quantized without any kind of noise shaping, the Signal-to-Noise Ratio (SNR) is approximated by the well-known formula

$$\text{SNR} \approx 6.02N + 10 \log_{10} \text{OSR} \quad [\text{dB}], \quad (2)$$

where N is the resolution of the quantizer, and $\text{OSR} = F_s/2B_s$ is the Oversampling Ratio.

Since in our case the SNR defined by (2) should be at least as large as the power density difference given by (1), it is straightforward to determine the needed number of bits from the -160 dBc/Hz out-of-band noise requirement. By taking into account the smallest possible OSR of the signal at the output of the interpolation chain for each LTE / LTE-A channel bandwidth, the minimum theoretical N lies between 12 and 13 bits. This result is confirmed by system-level simulations.

In a practical implementation, the digital word length used in the circuit should be larger than 13 bits, in order to leave sufficient room for the nonidealities of the RF front-end. In this DSP design, the adopted resolution is 16 bits.

C. Cubic Lagrange Interpolator

Since the overall interpolation ratio is not an integer number, a fractional interpolator is required in the circuit. In this work, the choice has fallen on a cubic Lagrange interpolation filter, because of its polynomial-based impulse response which enables efficient Farrow structure implementation [11].

The cubic Lagrange interpolator is the most complex block of our system, as it needs three hardware multipliers. Hence, in order to minimize power consumption, it should be clocked at the lowest possible frequency. This can be achieved by

- constraining the fractional interpolation factor F between 1 and 2, and
- keeping the sampling rate of the input signal to the Lagrange stage as low as possible, as explained next.

The continuous frequency response of an ideal cubic Lagrange interpolator is given by [12]

$$H_L(j\omega) = \left(1 + \frac{1}{6}\omega^2\right) \cdot \text{sinc}^4\left(\frac{\omega}{2}\right), \quad (3)$$

where ω is the angular frequency normalized to the input sampling rate, and $\text{sinc}(x) = \sin(x)/x$. Due to the *sinc*-like behavior of (3), the Lagrange interpolator needs an input signal with a fairly large pre-oversampling ratio, in order to provide acceptable image attenuation. System-level simulations showed that a pre-OSR of 4 (resulting in first image attenuation of at least 66 dB) is the minimum that guarantees to fulfill all the system requirements.

D. CIC Interpolator

The wide range of rate change factors required from the interpolation chain, spanning more than one order of magnitude, calls for a solution capable of supporting these large changes with minimum hardware overhead. One architecture fulfilling this criterion is the Cascaded Integrator-Comb (CIC) interpolator [13]. CIC filters have the further advantage that they do not require multiplications, making them suitable to running at high clock frequencies.

As shown in Fig. 2, a 3rd order CIC interpolator has been included as the final stage of the proposed interpolation chain. The rate change factor is normally calculated as $R = 2^{N_{CIC}}$, where N_{CIC} is the only integer for which the condition on the fractional interpolation factor $1 < F < 2$ is satisfied. Nevertheless, R can be selected to be any integer between 2 and 128. As will be illustrated in Section IV, this capability proves useful when the position of the interpolation images on the frequency spectrum needs to be changed.

At frequencies much lower than f_{out} , the response of the CIC block can be approximated by [13]

$$H_{CIC}(j\omega) \approx (2R \cdot \text{sinc}(\omega))^3, \quad (4)$$

where ω is again the angular frequency normalized to the low sampling rate. Because of the *sinc*-like nature of (4), similar pre-OSR considerations hold as for the cubic Lagrange interpolator. The pre-OSR to the CIC block ranges between 4 and 8 (depending on F), yielding first image attenuation between 62 and 81 dB. Section IV will prove that such a performance is good enough to fulfill the requirements.

E. Half-Band Filters

The increase in pre-OSR needed by the Lagrange and CIC interpolators is performed efficiently by two Half-Band (HB) filters as in [2], each interpolating by a factor of 2.

System-level simulations revealed that the minimum required stopband attenuations for the first and second HB filters are 80 and 100 dB respectively. This performance is achieved by using 55 and 19 taps. Because the impulse responses of

Fig. 3. If the first CIC image falls within the RX-band, the CIC rate change factor R can be decreased (from 8 to 6 in this case), while the fractional interpolation factor F is increased proportionally (in order to keep the product FR constant). This trick pushes the unwanted image to higher frequencies.

both filters are symmetrical, and about half of the coefficients are null, the actual number of implemented taps is reduced to 15 and 6.

IV. SYSTEM-LEVEL SIMULATIONS

In order to evaluate the system-level functionality of the presented approach, a model of the interpolation chain shown in Fig. 2 was implemented in MATLAB.

As stated in Section III, the CIC rate change factor R is usually constrained to be a power of 2. However, with some RF parameters, one of the images (for example from the CIC filter) may happen to fall exactly in the own RX-band, as shown in Fig. 3. This is handled by changing the value of R to a non-power-of-2 integer while proportionally adjusting the fractional interpolation factor F , in order to keep the ratio f_{out}/f_{in} unchanged. Such a simple trick allows to effectively remove the unwanted images from the RX-band.

The model of the presented interpolation chain was automatically tested by accounting for all possible LTE / LTE-A channel bandwidths and operating bands. Simulation results for both the Error Vector Magnitude (EVM) and Adjacent Channel Leakage Ratio (ACLR) show much better performance than what is to be expected at the overall TX output [9], [10]. This indicates that the impact of the DSP front-end on these parameters is negligible. On the other hand, by exploiting the flexibility described above, it is always possible to reduce the RX-band noise level below -160 dBc/Hz in all RF channel configurations.

V. DIGITAL SYNTHESIS

A VHDL behavioral model of the system was created and verified by comparison against the MATLAB model. Thereafter, the behavioral model was synthesized and place-and-routed in a 40nm low-power CMOS process, as well

Fig. 4. Estimation of the worst-case total power (cell internal + net switching + static leakage) consumed by the DSP front-end. The power numbers are calculated by considering the RF channel programming that causes the highest possible f_{out} for each channel bandwidth.

Fig. 5. Repartition of total power consumption among different blocks in the interpolation chain, with (a) 1.4 MHz LTE input signal, and (b) 20+20 MHz Carrier Aggregated (CA) LTE-A input signal. The areas marked as “others” include power dissipated by control logic, input and output interfaces, as well as part of the clock trees.

as timing analyzed to ensure correct circuit operation. The occupied core area of the resulting layout is 0.073 mm². RC parasitics and switching activities of the nets were extracted in order to reliably estimate power consumption.

The dissipated power varies widely depending on channel bandwidth and carrier frequency, because these quantities directly affect the clocking rates throughout the interpolation chain (through f_{in} and f_{out} , refer to Fig. 2). Fig. 4 shows the estimated total power consumption of the DSP front-end. The power numbers are calculated by considering the RF channel programming that causes the highest possible f_{out} for each channel bandwidth. Thereby, with different RF parameters these numbers will be always smaller. As an example, for the 1.4 MHz LTE signal the dissipated power can be as small as 6.3 mW if transmission occurs in Band 12, thus showing a 28% decrement with respect to the worst-case (8.8 mW when transmitting in Band 23).

The pie diagram of Fig. 5 illustrates how the total power is distributed among different circuit blocks. When the channel

TABLE I
SUMMARY OF THE DSP FRONT-END PERFORMANCE

EVM degradation	< 0.05%
ACLR	> 75 dB
RX-band noise	< -160 dBc/Hz
Core area	0.073 mm ²
Power consumption	6.3 ÷ 28.4 mW

bandwidth (and thus f_{in}) is small, most blocks are clocked at very low rate. Only the CIC interpolator has to operate at GHz frequencies, thus accounting for most of the dissipated power. On the other hand, when the channel bandwidth is large, all blocks need to work at fairly high clock rates, thus the power consumption is distributed more equally.

VI. CONCLUSION

In this paper, a digital interpolation chain for all-digital 4G transmitters is presented. A new architecture is proposed, where the number and order of blocks is optimized for high flexibility in the position of the digital images and wide non-integer interpolation factor range. The implemented circuit meets all system requirements with relatively small core area and low power consumption. These features make our system an ideal candidate for integration in future mobile handsets.

Table I summarizes the performance of the DSP front-end.

REFERENCES

- [1] J. Vankka *et al.*, “A GSM/EDGE/WCDMA modulator with on-chip D/A converter for base station,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2002, pp. 236–463.
- [2] M. Kosunen *et al.*, “A multicarrier QAM modulator for WCDMA base-station with on-chip D/A converter,” *IEEE Trans. VLSI Syst.*, vol. 13, no. 2, pp. 181–190, Feb. 2005.
- [3] P. Eloranta and P. Seppinen, “Direct-digital RF modulator IC in 0.13 μ m CMOS for wide-band multi-radio applications,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2005, pp. 532–615.
- [4] A. Jerng and C. Sodini, “A wideband $\Delta\Sigma$ digital-RF modulator for high data rate transmitters,” *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1710–1722, Aug. 2007.
- [5] N. Zimmermann *et al.*, “System architecture of an RF-DAC based multistandard transmitter,” in *52nd IEEE Int. Midwest Symp. Circuits and Systems*, Aug. 2009, pp. 248–251.
- [6] A. Pozsgay *et al.*, “A fully digital 65nm CMOS transmitter for the 2.4-to-2.7GHz WiFi/WiMAX bands using 5.4GHz $\Delta\Sigma$ RF DACs,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2008, pp. 360–619.
- [7] Z. Boos *et al.*, “A fully digital multimode polar transmitter employing 17b RF DAC in 3G mode,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2011, pp. 376–378.
- [8] *User Equipment (UE) radio transmission and reception*, 3GPP Std. TS 36.101, Rev. 11.3.0, Jan. 2013.
- [9] V. Giannini *et al.*, “A multiband LTE SAW-less modulator with -160 dBc/Hz RX-band noise in 40nm LP CMOS,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2011, pp. 374–376.
- [10] O. Oliaei *et al.*, “A multiband multimode transmitter without driver amplifier,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2012, pp. 164–166.
- [11] J. Ketola *et al.*, “Synchronization of fractional interval counter in non-integer ratio sample rate converters,” in *Proc. 2003 Int. Symp. Circuits and Systems*, May 2003, pp. 89–92.
- [12] A. Franck and K. Brandenburg, “A closed-form description for the continuous frequency response of Lagrange interpolators,” *IEEE Signal Process. Lett.*, vol. 16, no. 7, pp. 612–615, Jul. 2009.
- [13] E. Hogenauer, “An economical class of digital filters for decimation and interpolation,” *IEEE Trans. Acoust., Speech, Signal Process.*, vol. 29, no. 2, pp. 155–162, Apr. 1981.