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A Wideband Blocker-Resilient RF Front-End With Selective Input-Impedance Matching for Direct-$\Delta\Sigma$-Receiver Architectures

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Abstract—This paper presents a wideband blocker-tolerant RF front-end suitable for direct-$\Delta\Sigma$-receivers. Blockers are attenuated by providing low receiver input impedance at blocker frequencies while for desired frequency the input impedance is boosted to matched condition by providing an up-converted positive feedback from the baseband stage. RF front-end is evaluated on 28nm fully-depleted silicon-on-insulator CMOS process with current consumption of 8mA, excluding local-oscillator drive, at 1V supply voltage. Front-end is reconfigurable from 0.7-3GHz with maximum noise figure of 5dB and achieves an out-of-band 1dB compression point of 0dBm at 100MHz local oscillator frequency offset.

I. Introduction

In order to efficiently utilize the frequency allocation spectrum of emerging radio access standards such as 5G and LTE-A, a reconfigurable wideband RF-to-digital receiver is needed. With reconfigurable design, RF-to-digital receivers are promising replacement of existing transceiver designs dedicated for a certain standard. One relatively new digital intensive architecture is direct-$\Delta\Sigma$-receiver (DDSR) as illustrated in Figure 1. This architecture was introduced in [1] and is a further step towards a full RF-to-digital converter. The architecture is based on direct downconversion delta-sigma feedback that is directly up-converted to RF nodes through application of N-path filtering technique. Thus core receiver functionality of channel filtering and delta-sigma quantization noise shaping already begins at RF. In other words, the receiver performs the channel filtering, signal downconversion and quantization noise shaping simultaneously.

In this paper we propose a blocker resilient RF front-end suitable for DDSR applications. Inherently, such DDSR receivers are exposed to high-power out-of-band (OB) blocker signals. If not attenuated, these blockers can completely saturate the receiver input and make the receiver operation non-linear. Our front-end achieves this blocker attenuation by creating a low RF front-end input impedance at blocker frequencies while for the desired channel the input impedance is boosted to matched condition by an up-converted positive feedback from baseband (BB) as depicted in Figure 2.
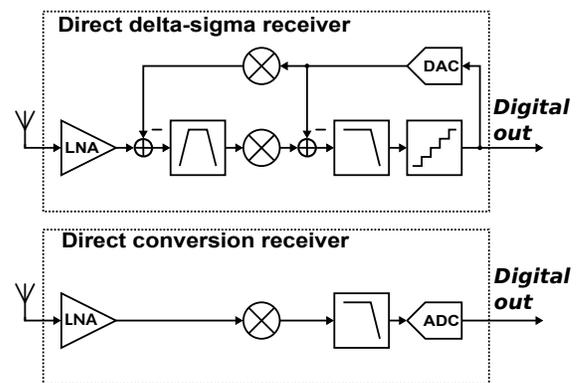

Fig. 1. Conceptual comparison between a direct conversion receiver and direct $\Delta\Sigma$ receiver

The paper is organized such that Section II describes the prior art related to blocker tolerant receivers. Section III discusses proposed RF front-end architecture while Section IV details the circuit implementation of proposed architecture. Paper concludes with receiver simulation results and conclusion.

II. Prior Art:Blocker-Tolerant RF Front-Ends

A number of innovative ideas such as applying N-path filtering to improve RF front-end blocker resilience, have been demonstrated earlier [2], [3]. However, in most cases, the basic first order N-path filtering technique is inadequate for stringent OB blocker rejection demands of recent mobile communication standards. Another technique to attenuate blockers is to minimize voltage gain at RF frequencies by employing low-noise-transconductance-amplifiers (LNTA's) or mixer first receiver arrangement [2], [4]–[6]. Receivers employing LNTAs or mixer first topologies shift almost all the gain to baseband stages where it is easier to implement selective on-chip filtering for suppression of OB blockers. Reduced gain at RF frequencies results in more linear RF front end.
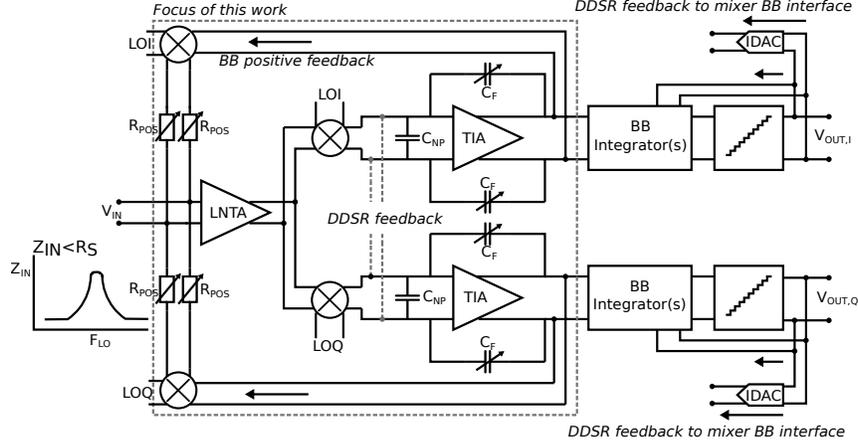
Fig. 2. Proposed wide-band DDSR architecture. Blockers are attenuated through low Zin of LNTA while positive feedback from BB increases the Zin for desired frequency

Among LNTA and mixer first topologies, mixer first topology is sensitive for LO emissions. In the DDSR concept the LO emissions become even more problematic due to wideband quantization noise images from the DDSR feedback at RF nodes [1].Thus, a mixer first topology is not optimum for our application. On the other hand, LNTA topology is promising as it isolates the RF nodes from the antenna and provides better in-band linearity. However, LNTA based receivers reduce blocker gain only at LNTA output node(s) and fail to address that the input transconductor can also go into non-linear operation if the input signal reaches the input swing limitation of input transconductor. In order not to cause any non-linearity due to LNTA input swing limitations, ideally, blocker gain suppression should already occur at earliest point in receiver chain, which is the LNTA input.

Based on aforementioned discussion, our solution is based on a low intrinsic input impedance LNTA structure, which has been enhanced with a positive feedback from BB to match the front-end input impedance only at desired frequencies. Positive feedback from BB idea has been demonstrated earlier in [5], [7] for LNA and mixer first receivers. However, as per author's knowledge, this is the first paper where an LNTA is merged with positive feedback from BB.

III. RF FRONT-END FOR DDSR

Figure 2 shows the block diagram of proposed LNTA based DDSR front-end. LNTA intrinsic input impedance is designed to be low for OB blocker signals while for the desired frequency input impedance is boosted to match source impedance R_S through implementation of up-converted positive feedback from BB. The feedback path is selective due to low-pass filtering characteristics of BB and therefore only increases the input impedance at desired frequency. The overall receiver input impedance of LNTA can then be found as:

$$Z_{IN}(F_{LO}) = \frac{Z_{LNTA}}{1 - A_{loop}}$$

where Z_{IN} is the input impedance of RF front-end at desired LO frequency, Z_{LNTA} is the intrinsic input impedance of the LNTA and A_{loop} is the loop-gain of the feedback structure. If we assume relatively small voltage gain of LNTA in comparison to BB stage, LNTA gain can then be ignored and overall A_{loop} can be given as:

$$A_{loop} = \gamma.Z_{TIA}.(\frac{Z_{IN}}{Z_{IN} + R_{POS}})$$

where Z_{TIA} denotes the transimpedance of BB transimpedance amplifier (TIA) and γ represents passive mixer conversion losses. By adjusting the value of R_{POS}, loop gain of the feedback structure can be changed and consequently the input impedance of RF front-end can be controlled. Relative attenuation (AT) of blocker, which is dependent on the ratio of Z_{LNTA} and R_S can be given as [7]:

$$AT(dB) = -20log(\frac{R_S + Z_{LNTA}}{Z_{LNTA}})$$

Due to square wave LO signal, up-converted positive feedback will also occur at the harmonics of LO frequency. This will increase the LNTA input impedance at LO harmonics as well. Therefore, any blockers present exactly at LO harmonics will not be attenuated through selective voltage attenuation. Feedback at LO harmonics can be reduced using harmonic rejection mixer arrangements.

IV. FRONT-END DESIGN

Front-end LNTA implementation consists of parallel combination of common-gate (CG) and push-pull common-source (CS) amplifiers as depicted in Figure 3 [8]. This parallel combination increases the LNTA tranconductance g_m and push-pull configuration helps to achieve better large signal linearity. Furthermore, to maximize output voltage swing range, output common-mode voltage is set to half of supply voltage by implementing a common-mode feedback loop. Differential intrinsic input impedance of LNTA was designed to be around
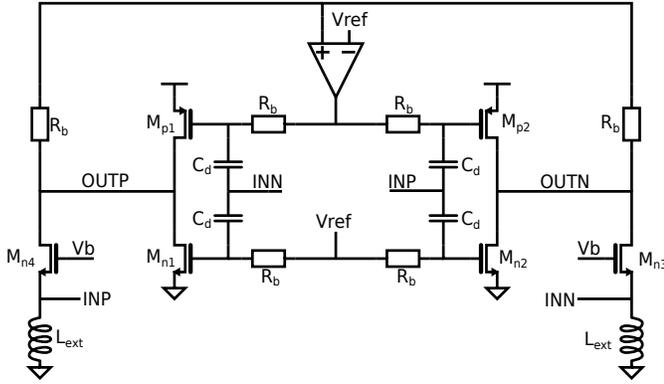
Fig. 3. Designed common gate-common source LNTA for proposed receiver architecture.

Fig. 4. Z_{IN} of proposed RF front-end. LNTA provides around 25Ω Zin for far away blockers

25Ω by increasing the CG g_m to be about 45mS. Designed LNTA consumes 8mA at 1V supply with small signal g_m value of 75mS.

Positive feedback from the output of BB TIA is up-converted to RF nodes through passive N-path filtering. Amount of positive feedback is controlled through series resistors R_{POS}. Positive feedback systems have a potential risk of instability. To ensure stability, a simplified s-plane transfer function for front-end was derived using [9] and stability of front-end was checked for different values of R_{POS} through pole-zero plots. Pole-zero plots and transient analysis both confirmed front-end stability for $R_{POS} > 4K\Omega$. In designed circuit value of R_{POS} is set at $4.5K\Omega$.

Transistors with large width-to-length ratio of $48/0.03\mu m$ were implemented in main path mixers. This ensured a small switch resistance of 8Ω for better attenuation at far away offsets from LO. Feedback capacitor C_F across the BB TIA stage forms a first order low pass filter network blocking the OB frequencies. Capacitor C_{NP} of 10pF was added at the mixer-BB interface to further attenuate OB blockers. The proposed RF front-end can also be designed with a higher-order low-pass filter response for BB such as in [6]. This will help to further attenuate near-band blocker frequencies.

V. PERFORMANCE EVALUATION

Proposed front-end was simulated in 28nm fully-depleted silicon-on-insulator (FDSOI) process with 1V supply voltage. front-end is reconfigurable from 0.7-3GHz with a BB band-width of 10MHz. For this work, designing a complete DDSR receiver was out-of-scope. Therefore, for concept demonstration, a single stage BB gain stage was designed with ideal DDSR feedback provided at mixer-BB interface. TIA was designed with a self-biased differential pair and current consumption of 3.8mA. Further, based on our previous implementation [10], estimated values of PCB and layout parasitics, pad capacitances,bondwire inductances and s-parameter models of 20nH off-chip RF-chokes (L_{ext}) were added in order to match the simulated results more closely to the real scenario.

Figure 4 shows the simulated differential input impedance of about 25Ω for blocker frequencies. At higher frequencies,
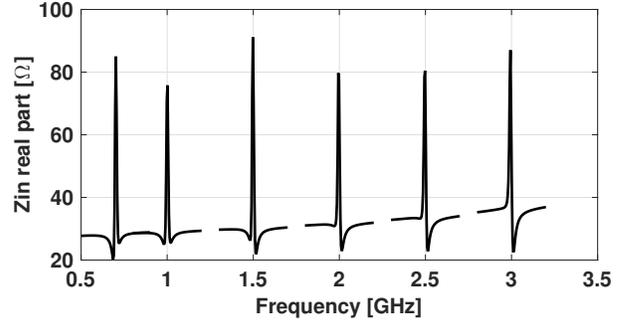
however, effect of bond-wire inductance increases the input impedance to be somewhat higher. Figure 5 shows the simulated gain and S11 of proposed circuit. Response shows a receiver gain of 40-45dB from 0.7GHz to 3GHz for the desired 20MHz RF bandwidth.

As depicted in Figure 2, an ideal DDSR negative feedback to mixer-BB interface brings down the voltage gain at these nodes. This causes front-end amplifier to operate in LNTA mode. However, due to limited mixer switch resistance, load impedance seen by LNTA can not reach zero. This results in couple of dB voltage gain at RF frequencies as well. Moreover, positive feedback from BB to LNTA input nodes also increases the voltage gain of LNTA at desired frequencies. Therefore, in the designed circuit, a compromise was made between low LNTA voltage gain and input matching, by only giving minimum possible positive feedback for input matching so that the voltage gain is kept below 10dB at desired band.

Figures 6 and 7 shows the simulated 1dB blocker compression point (OB P1dB) and NF simulations for the whole receiver and RF front end. RF front-end achieves an OB P1dB of 0dBm at 100MHz offset from the LO frequency with maximum receiver integrated NF of 5dB. It can be seen from Figure 6 that the overall receiver OB P1dB is worse than RF front-end linearity. This is due a simple one stage design of BB TIA which uses first order filtering for blocker attenuation. For more linear BB performance, the BB gain can be divided into stages with individual first-order responses.

VI. CONCLUSION

Emerging wideband RF-to-digital receivers need to operate under the presence of strong OB blockers. These blockers can cause receiver input amplifiers to saturate and therefore make the receiver non-linear. This paper proposed an RF front-end solution for DDSR, consisting of a low intrinsic input impedance LNTA, which avoids the blocker voltage gain at LNTA input and output node(s). This ensures that the voltage swing limitations are not reached even with strong blocker signals. For desired frequency, input impedance is increased to matched condition through a positive up-converted feedback from BB. Simulated results show a OB-P1dB point of 0 dBm at 100MHz offset from the desired center frequency

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work[4]	[5]	[10]	[1]	[11]
Architecture	LNTA first DDSR	LNTA first DDSR	LNA first DDSR	LNA first DDSR	LNTA first
Process	28nm FDSOI	65nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS
Supply voltage (V)	1	1.2	1.1	1.2	1.2
BB bandwidth (MHz)	10	10	15	28	10
Carrier Frequency (GHz)	0.7-3	0.6-3	0.7-2.7	0.9	0.7-3.8
Gain (dB)	9 (Front-end) 42 (Receiver)	50	-	40	42
Noise Figure (dB)	4.5-5	2.4-3.5	5.9-8.8	6.2	1.6-3.2
Blocker input P1dB (dBm)	0[1](Front-end) -10[1] (Receiver)	-20[1]	-12[2]	-18[3]	-18[1]

1) Blocker at 100MHz offset, 2) Blocker at 92.5MHz offset, 3) Blocker at 80MHz offset, 4) Simulated response
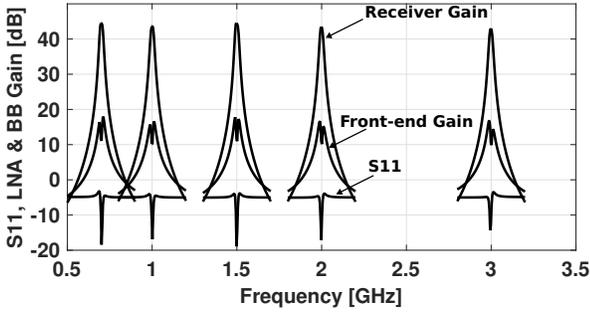

Fig. 5. Simulated S11, RF and BB Gain for the proposed receiver at five operating frequency settings.
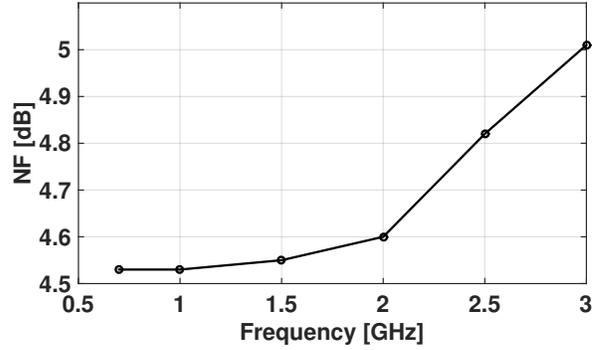

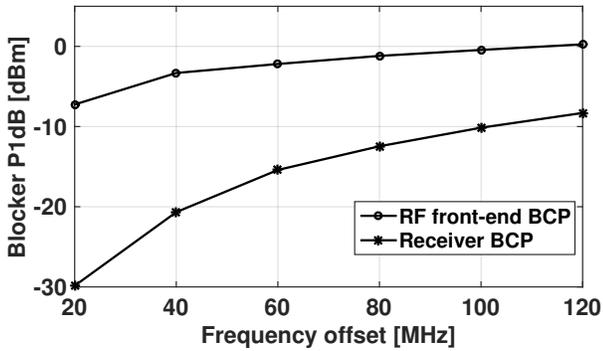Fig. 7. Receiver noise figure across operating band.

Fig. 6. Blocker compression point for the proposed receiver at 1.5GHz

with maximum NF of 5dB. Results collected into Table 1 indicate the proposed approach is able to achieve state-of-the art blocker tolerance even with lower supply voltage and one baseband gain stage design.

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