This is an electronic reprint of the original article.
This reprint may differ from the original in pagination and typographic detail.

Haapala, Tuomas; Halonen, Kari

A Fully Integrated Digitally Programmable Pulse Shaping 6.0-8.5 GHz UWB IR Transmitter Front-End for Energy Harvesting Applications

Published in:
2018 IEEE International Symposium on Circuits and Systems (ISCAS)

DOI:
[10.1109/ISCAS.2018.8350895](https://doi.org/10.1109/ISCAS.2018.8350895)

Published: 01/01/2018

Document Version
Peer reviewed version

Please cite the original version:
Haapala, T., & Halonen, K. (2018). A Fully Integrated Digitally Programmable Pulse Shaping 6.0-8.5 GHz UWB IR Transmitter Front-End for Energy Harvesting Applications. In *2018 IEEE International Symposium on Circuits and Systems (ISCAS)* (pp. 1-5). (IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS PROCEEDINGS). IEEE. <https://doi.org/10.1109/ISCAS.2018.8350895>

This material is protected by copyright and other intellectual property rights, and duplication or sale of all or part of any of the repository collections is not permitted, except that material may be duplicated by you for your research use or educational purposes in electronic or print form. You must obtain permission for any other use. Electronic or print copies may not be offered, whether for sale or otherwise to anyone who is not an authorised user.

A Fully Integrated Digitally Programmable Pulse Shaping 6.0-8.5 GHz UWB IR Transmitter Front-End for Energy Harvesting Applications

Tuomas Haapala, Kari Halonen

SMARAD-2/Department of Electronics and Nanoengineering, Aalto University School of Electrical Engineering, Espoo, Finland

Email: firstname.lastname@aalto.fi

Abstract—This paper presents a fully integrated ultra-wideband impulse radio transmitter front-end (TFE) that is compliant with the European spectral mask. The compliance is achieved by means of 4-bit digital pulse shaping and an integrated matching network. The center frequency of the TFE is digitally tunable with 24 MHz resolution between 6.5 - 8.0 GHz. The TFE delivers at least 2.0 pJ pulses over the whole frequency range and achieves 4.4 % efficiency at 7.5 GHz center frequency and 4 MHz pulse repetition rate. The static power consumption is 480 nW, which enables the TFE to reach high efficiency levels even at low pulse repetition rates. The TFE is designed in a commercial 65-nm CMOS process. The performance of the TFE is evaluated through post-layout simulations.

I. INTRODUCTION

Many internet of things scenarios predict an exponentially growing number of ambient sensors for the near future. To avoid extensive wiring, many of these sensors are made capable of wireless data transfer. In addition, some of these wireless sensors employ energy harvesting to limit the number of batteries that would eventually require replacing.

Ultra-wideband impulse radios (UWB IRs) have been proposed as a potential candidate for realizing wireless capabilities for energy-autonomous sensor nodes [1], [2]. Most recently published low-power UWB IRs target the U.S. UWB mask between 3.1 – 4.8 GHz, regulated by the Federal Communication Commission (FCC). This allows power savings due to low center frequency and relaxed spectral requirements compared to Asia and Europe. However, UWB IRs designed for the FCC mask rarely comply with the regulations of other regions due to the relaxed requirements, which limits the global applicability of these designs. In addition, most regions only allow usage of the 3.1 – 4.8 GHz frequency range presuming appliance of mitigation techniques [3]. The band is also surrounded by strong narrow-band ISM and WLAN interferers, which makes receiver design more challenging.

Edge-combining IR UWB transmitters have demonstrated adequate pulse shaping (PS) capabilities for potential compliance with the European (EC) UWB mask [4]. However, edge combiners based on a delay chain often suffer from coarse digital frequency tuning resolution [4]–[7] or they rely on analog frequency tuning [8].

Fig. 1. Edge-combining TFE architecture. The TFE consists of delay units (Δ), routers (R), combiners (C), a power amplifier (PA) and a matching network (MN).

This work presents a fully integrated edge-combining UWB IR transmitter front-end (TFE) that complies with the EC UWB mask [9] between 6.0 - 8.5 GHz up to moderate pulse repetition rates (PRRs). The compliance is achieved by means of 4-bit pulse-shaping and an integrated matching network. The frequency band above 7.25 GHz has a wide unrestricted global availability [3]. In addition, the TFE demonstrates a novel digital center frequency (f_c) tuning method based on switchable supply capacitor banks that shows an excellent linearity over a wide tuning range and a high tuning resolution. The TFE demonstrates a very low static power consumption level that allows high-efficiency operation also at low PRRs. The generated pulse energy level suffices for a line-of-sight communication range of more than ten meters with a high-quality receiver [2], [7].

II. IMPLEMENTATION

A block-level description of the designed impulse-combining TFE architecture is presented in Fig. 1. There are 32 programmable delay units (Δ) forming a delay chain. The propagation delay δ over a single unit is translated into the equivalent pulse center frequency by approximation $f_c \approx \frac{1}{\delta}$. Each delay unit delivers an impulse to a router (R). The router propagates the input impulse to up to 4 parallel output channels based on a 4-bit tuning word. Each router is independently programmable and defines the 4-bit amplitude setting of a single sub-pulse of the final output waveform. The

Fig. 2. Isolated delay unit supply control. (a) Digitally tunable supply capacitor bank. (b) Transient behavior of an isolated supply voltage $V_{dd\Delta}$ of a delay cell during pulse generation.

impulses propagated by the routers are serialized by parallel-to-series (PTS) converters α and β that consist of impulse combiners (C). The delay chain delivers alternate impulses to PTS converter α and the rest to β . This interleaving relaxes the speed requirement of the combiners. Finally, the generated trains of serial impulses trigger the power amplifier (PA) that has an integrated matching network (MN).

A. Digitally tunable delay unit

The applied delay units are similar to the implementation in [7]. The delay unit propagates and reloads fast, allowing a high maximum center frequency and a high maximum PRR. Instead of using programmable driver transistors [4], [5], programmable capacitive loading [6] or analog supply voltage control [8], however, we propose adjusting the propagation delay of the delay units by altering their supply voltage level by means of a digitally programmable capacitor bank. Based on simulations, some advantages of the proposed method include high linearity and a wide tuning range.

A gradual drop in the supply level of the delay units during pulse generation will translate into an increased δ (decreased f_c) along the delay chain. For this reason, the power supply of an edge-combining impulse transmitter needs extensive buffering especially in energy harvesting applications where the applied harvester cannot necessarily provide high current levels. To relieve supply buffering requirements, we propose giving each delay unit an isolated supply. Since every delay unit is triggered only once per generated pulse, the isolated supply voltages can drop significantly during trigger propagation while the TFE still retains a constant δ along the delay chain.

The isolated supply of a delay unit, $V_{dd\Delta}$, is created by a capacitor bank as presented in Fig. 2(a). Capacitor C_0 provides a low-resistance energy buffer for the delay unit. Initially, switches S_1 are open and switches S_3 connected to either V_{dd} (1.2 V) or V_{dd2} (0.6 V), charging unit capacitors C_u through switches S_2 . The position of switches S_3 is controlled by binary control word *tune_freq*. Capacitor C_0 is charged to V_{dd} through a separate switch (not shown in Fig. 2(a)). During pulse generation, switches S_2 are opened and switches S_1 then closed, connecting unit capacitors C_u and capacitor C_0 in parallel. The consequent charge distribution between the

Fig. 3. Building blocks for the TFE. (a) High-speed router and impulse combiner. (b) Power amplifier. (c) Matching network.

capacitors sets the targeted $V_{dd\Delta}$ level. The capacitor bank is returned back to the initial state after pulse generation.

A transient simulation of the behavior of $V_{dd\Delta}$ during pulse generation is shown in Figure 2(b). It also shows the control voltages for switches S_1 and S_2 , a low control voltage level denoting a closed switch. Initially, capacitor C_0 is charged to V_{dd} . $V_{dd\Delta}$ has settled to its target level at about 2 ns. The delay unit is triggered at around 4.5 ns, resulting in consumed charge and a consequent drop in $V_{dd\Delta}$. The capacitor bank is recharged immediately after pulse generation.

The final implementation uses binary 5-bit capacitor banks ($C_u = 33$ fF) for coarse $V_{dd\Delta}$ tuning and binary 4-bit capacitor banks ($C_u = 2.1$ fF) for fine $V_{dd\Delta}$ tuning.

B. Other blocks

Fig. 3(a) shows the implementation of the routers and combiners. The routers are based on two cascaded inverters, the transparency of the former being controlled by a switch transistor. A single router comprises 4 inverter pairs that constitute the 4 output channels. The combiners convert 4 parallel input impulses into a single output impulse. An impulse at the gate of one of the input transistors M1 – M4 pulls node 1 low, which results in the output node being pulled high by inverter I1. The feedback path composed of inverter I2 and transistor M5 return node 1 back to its original state, after which the output is also returned low. Transistor M6 keeps node 1 pulled high at the steady state. The proposed combiner propagates fast since it does not include any cascaded transistors. In addition, the combiners have a small input capacitance.

The PA design is shown in Fig. 3(b). It has 4 input channels, each of which is divided to 2 sub-channels for impulse trains coming from PTS converters α and β . After buffering, the impulse trains are combined at the drain of the PA. Fig. 3(c) shows the schematic of the fully integrated wideband MN. The MN consists of an elliptic low-pass section (enclosed

Fig. 4. Performance of the matching network. PL = Post-layout simulation, EM = electromagnetic simulation, Real = real part of Z_L , Imag = imaginary part of Z_L . (a) Forward transmission coefficient S_{21} . (b) Load impedance Z_L . (c) Group delay τ .

by the dashed rectangle) and a simple band-pass section that is also used to bias the PA drain with supply voltage V_{dd2} . Capacitor C_1 includes the output capacitance of the PA drain and capacitor C_5 includes the parasitic capacitance of the output pad. The load impedance seen by the PA drain (Z_L) is converted by a capacitive Norton transformation of capacitor C_3 that down-converts the impedance on its left [10]. The real part of Z_L is set to approximately 30Ω based on simulations as a trade-off between maximum output energy and linearity.

III. SIMULATION RESULTS

The TFE was designed using a commercial triple-Vt 65-nm CMOS process and validated through post-layout (PL) simulations in Spectre. In addition, the MN was analyzed and adjusted through electromagnetic (EM) simulations in Momentum. The TFE measures $240 \mu\text{m} \times 340 \mu\text{m}$ including the delay chain supply capacitor banks but excluding the PA and MN. The PA and MN measure $280 \mu\text{m} \times 470 \mu\text{m}$.

Simulation results for the MN are presented in Fig. 4. Fig. 4(a) is normalized to 50Ω . The -1 dB passband of the MN ranges from 5.7 GHz to 9.1 GHz. In that range, the real part of Z_L is matched to approximately 30Ω while the imaginary part remains small. The minimum attenuation in the passband is 2.4 dB. Between 6.5 - 8.0 GHz, the maximum group delay variation over a 500 MHz band is less than 10 ps.

The full f_c tuning range of the TFE is shown in Fig. 5(a). Here, f_c is given by the inverse of the average propagation delay over a single delay unit. The target f_c band between 6.5 - 8.0 GHz is fully covered at tt, ss and ff process corners over the temperature range from -40 to 80 °C.

Fig. 5. Frequency tunability of the TFE. (a) Full frequency tuning range. (b) Fine frequency tuning resolution.

Fig. 6. Pulse shaping (PS) performance. (a) Pulse energy E_p and energy consumption E_c as a function of f_c . (b) Large and small energy Gaussian pulse envelopes. (c) Spectra of 4 MHz PRR pulse trains at the four target sub-bands with 2.1 pJ pulse energy. The EC UWB mask [9] (generic, with no mitigation techniques applied) is shown dashed.

A Monte Carlo (MC) simulation of the fine frequency tuning resolution of the delay chain is presented in Fig. 5(b). The data consists of 32 MC points at tt corner, each of which comprises 15 fine tuning steps in the middle of the full tuning range (480 steps in total). TFE has an average fine frequency tuning resolution of 19.6 MHz with a 1.2 MHz standard deviation (σ). The equivalent voltage step is 0.76 mV. A 64-point MC simulation in the middle of the tuning range gives an average coarse tuning step of 218 MHz with a 1.5 MHz standard deviation.

The PS performance of the TFE is depicted in Fig. 6. The TFE is programmed with a Gaussian envelope of constant pulse length that results in a 500-MHz signal bandwidth. The four target sub-bands are centered at 6.5, 7.0, 7.5 and 8.0 GHz.

TABLE I
COMPARISON WITH THE STATE OF THE ART.

	This work (simulated)	Vauche [8] TCAS-I 2017	Miranda [4] CICC 2010	Solda [11] JSSC 2011	Huang [12] JSSC 2013	de Steel [2] JSSC 2017	Dokania [13] TCAS-II 2010
CMOS tech. (nm)	65	130	65	130	180 BiCMOS	28 FDSOI	90
Type	Edge-combiner	Edge-combiner	Edge-combiner	LO-based	LO-based	LO-based	LO-based
Mask	EC	FCC	FCC	FCC	FCC	FCC	FCC
f_c range (GHz)	6.5 – 8.0	3 – 5	3.6 – 7.5	6.6 – 9.0	7.5 – 12.2	3.5 – 4.5	3.5 – 4.5
f_c resolution (MHz)	23	Analog	1000	80	n.a.	n.a.	Analog
PS resolution (bits)	4	Analog	3	0	1	5	1
P_s (μ W)	0.48	100	13	n.a.	0.00017	n.a.	5
PRR (MHz) f_c (GHz)	4 7.5	1 4	12 3.6	5 7.5	0.03 9.8	6.81 4.5	0.1 3.5
E_p^* (pJ)	2.1	0.64	2.4*	13.2	1.5 [†]	0.64	1.0 [†]
E_c^* (pJ)	48	250	9.6*	186	747	30	80
η^* (%)	4.4	0.26	25*	7	0.2 [†]	2.1	1.3 [†]

* At the conditions defined by PRR (MHz) | f_c (GHz) column. * Estimated from Fig. 5 at 0.75 V antenna driver voltage. [†] Estimated based on the reported pulse waveform.

Fig. 6(a) shows that the TFE generates a constant output pulse energy over the target f_c range. More energy is consumed per pulse (E_c) at higher frequencies since more impulse combinations (sub-pulses) are required for pulse generation. At a 2.1 pJ pulse energy (E_p) and 7.5 GHz f_c setting, the TFE consumes 48 pJ per pulse, corresponding to 4.4 % efficiency (η). The static power consumption (P_s) is 480 nW.

The maximum PRR of the TFE is about 25 MHz at ss corner, limited by the reload time of the delay chain supply capacitor banks. However, the maximum continuous PRR is limited by the spectral quality of transmission. Example pulse envelopes at 7.5-GHz f_c are shown in Fig. 6(b). At medium E_p levels around 2 pJ, the mask is violated by the main lobes at 4 MHz PRR. The power spectral densities (PSDs) of four 2 pJ output pulse trains at 4 MHz PRR at the target sub-bands is shown in Fig. 6(c).

IV. COMPARISON WITH OTHER WORKS

The performance of the TFE is compared with the current state of the art in Table I. The selected works have been verified by measurements and combine a high E_p level with a low or moderate PRR option. The TFE is set to 7.5 GHz f_c for a wide global availability.

The proposed TFE is the only one to target the EC UWB mask. Despite the more strict spectral requirements, the integrated matching network and a high f_c , the TFE achieves a comparable E_p and η . The novel f_c tuning method achieves a better resolution than most designs. Fig. 7 demonstrates how the TFE retains a very low power consumption level over a wide range of PRRs due to its low P_s level. This feature is practical in energy harvesting applications where the acquirable power level may vary from microwatts to milliwatts depending on ambient conditions and harvester size. While the transmitters in [7], [15] and [16] demonstrate a slightly lower power consumption, they operate at the low FCC band, suffer from coarse frequency tuning and lack PS capabilities.

V. CONCLUSION

This paper presents a fully integrated UWB IR TFE whose performance was evaluated through post-layout simulations.

Fig. 7. Comparison with other UWB IR Tx designs of similar characteristics. The TFE is set to 2.1 pJ E_p and 7.5 GHz f_c . All the other shown designs target the FCC mask.

The compliance with the EC UWB mask is achieved by means of 4-bit pulse shaping and an integrated PA matching network. Unlike designs targeting the FCC UWB mask, this design has a wide global applicability. The TFE delivers 2.1 pJ pulses at 7.5 GHz center frequency with 4.4 % total efficiency, demonstrating a comparable performance to the state of the art. The novel digital f_c tuning method based on isolated supply capacitor banks allows a wide tuning range with an improved tuning resolution of 24 MHz between 6.5 – 8.0 GHz. The P_s is 480 nW, allowing a high efficiency level even at low data rates. The low P_s level and the isolated supply capacitor banks improve the practicality of the design in energy harvesting applications.

ACKNOWLEDGMENT

This work was funded by The Naked Approach (40336/14, 3246/31/2014) and Towards Digital Paradise (2727/31/2016) projects granted by Business Finland, EffiNano project granted by Aalto University School of Electrical Engineering (10/2012, 1/2014) and Aalto ELEC Doctoral School. The authors thank Tuomas Rantataro, Mika Pulkkinen and Jarno Salomaa for their technical advice.

REFERENCES

- [1] J. Kang et al., "Design and Optimization of Area-Constrained Wirelessly Powered CMOS UWB SoC for Localization Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 4, pp. 1042-1054, April 2016.
- [2] G. de Streel et al., "SleepTalker: A ULV 802.15.4a IR-UWB Transmitter SoC in 28-nm FDSOI Achieving 14 pJ/b at 27 Mb/s With Channel Selection Based on Adaptive FBB and Digitally Programmable Pulse Shaping," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1163-1177, April 2017.
- [3] J. R. Fernandes and D. Wentzloff, "Recent advances in IR-UWB transceivers: An overview," in *Proc. IEEE International Symposium on Circuits and Systems*, 2010, pp. 3284-3287.
- [4] H. Miranda and T. H. Meng, "A programmable pulse UWB transmitter with 34% energy efficiency for multichannel neuro-recording systems," in *Proc. IEEE Custom Integrated Circuits Conference*, 2010, pp. 1-4.
- [5] A. Ebrahah and P. Mohseni, "30 pJ/b, 67 Mbps, Centimeter-to-Meter Range Data Telemetry With an IR-UWB Wireless Link," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 9, no. 3, pp. 362-369, June 2015.
- [6] K. Na et al., "A 200-Mb/s Data Rate 3.1-4.8-GHz IR-UWB All-Digital Pulse Generator With DB-BPSK Modulation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 12, pp. 1184-1188, Dec. 2015.
- [7] T. Haapala et al., "A 180-nW static power UWB IR transmitter front-end for energy harvesting applications," in *Proc. IEEE International Symposium on Circuits and Systems*, 2017, pp. 2347-2350.
- [8] R. Vauche et al., "A 100 MHz PRF IR-UWB CMOS Transceiver With Pulse Shaping Capabilities and Peak Voltage Detector," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 6, pp. 1612-1625, June 2017.
- [9] European Commission, "Commission Decision 2014/702/EU of 7 October 2014 amending Decision 2007/131/EC on allowing the use of the radio spectrum for equipment using ultra-wideband technology in a harmonised manner in the Community," 2014/702/EU, Oct. 2014.
- [10] L. Besser and R. Gilmore, *Practical RF Circuit Design for Modern Wireless Systems, Vol. 1: Passive Circuits and Systems*, Norwood, MA: Artech House, 2003.
- [11] S. Solda et al., "A 5 Mb/s UWB-IR Transceiver Front-End for Wireless Sensor Networks in 0.13 μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1636-1647, July 2011.
- [12] K. K. Huang et al., "An Ultra-Low-Power 9.8 GHz Crystal-Less UWB Transceiver With Digital Baseband Integrated in 0.18 μm BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3178-3189, Dec. 2013.
- [13] R. Dokania et al., "An Ultralow-Power Dual-Band UWB Impulse Radio," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 7, pp. 541-545, July 2010.
- [14] F. Padovan et al., "A 20Mb/s, 2.76 pJ/b UWB impulse radio TX with 11.7% efficiency in 130 nm CMOS," in *Proc. IEEE European Solid State Circuits Conference*, 2014, pp. 287-290.
- [15] O. Z. Batur et al., "An Ultra Low-Power Dual-Band IR-UWB Transmitter in 130-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 11, pp. 701-705, Nov. 2012.
- [16] S. Gambini et al., "A Fully Integrated, 290 pJ/bit UWB Dual-Mode Transceiver for cm-Range Wireless Interconnects," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 3, pp. 586-598, March 2012.