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Published in:
IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS

DOI:
[10.1109/TCSI.2016.2529280](https://doi.org/10.1109/TCSI.2016.2529280)

Published: 23/03/2016

Document Version
Peer reviewed version

Please cite the original version:
Lemberg, J., Kosunen, M., Roverato, E., Martelius, M., Stadius, K., Anttila, L., Valkama, M., & Ryyänen, J. (2016). Digital Interpolating Phase Modulator for Wideband Outphasing Transmitters. *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS*, 63(5), 705-715 .
<https://doi.org/10.1109/TCSI.2016.2529280>

Digital Interpolating Phase Modulator for Wideband Outphasing Transmitters

Jerry Lemberg, Marko Kosunen, *Member, IEEE*, Enrico Roverato, *Student Member, IEEE*, Mikko Martelius, Kari Stadius, *Member, IEEE*, Lauri Anttila, *Member, IEEE*, Mikko Valkama, *Senior Member, IEEE*, and Jussi Ryyänen, *Member, IEEE*

Abstract—Radio transmitters are evolving towards digital-intensive solutions to exploit reconfigurability and benefit from CMOS process scaling. Outphasing has been identified as a suitable candidate for digital wideband transmitters. However, with recent digital-intensive outphasing transmitters the achieved performance in terms of adjacent channel leakage ratio (ACLR) has been limited. This paper identifies the sampling images of the modulating phase signal as the main factor limiting the ACLR of digital outphasing transmitters. We present a new digital interpolating phase modulator architecture, capable of providing significantly better sampling image attenuation. When evaluated in outphasing configuration with a 100 MHz OFDM signal at the carrier frequency of 2.46 GHz, and 10-bit phase resolution, the proposed solution achieves an ACLR of -59 dBc, compared to -43 dBc achievable with the phase modulator architecture utilized in state-of-the-art digital outphasing transmitters. The proposed digital interpolating phase modulator is also capable of custom carrier generation, a straightforward method for generating an arbitrary carrier frequency up to 1.25 times the phase modulator sampling rate.

Index Terms—Outphasing, digital, transmitter, interpolation, phase modulator, DIPM, custom carrier generation, CCG, linearity, ACLR.

I. INTRODUCTION

THE ever growing demand for higher data rates in wireless communication can only be met by improving spectral efficiency. The complex modulation schemes and wide bandwidths already in use today set stringent requirements for the radio transmitter. Especially in mobile cellular radio systems it is typical for the base station to transmit modulated carriers of different network operators and even different network technologies with common hardware. Thus, this combination of reconfigurability and linearity requirements set for multi-standard transmitters is best met with digital-intensive solutions. Therefore, the trend in transmitters has been to push the D/A-conversion as close to the antenna as possible.

The first digital-intensive transmitter architectures targeted for wideband operation were based on the RF-DAC concept

[1], [2]. Several Cartesian [3]–[8] and polar [9]–[12] transmitters based on high amplitude resolution RF-DACs have since been reported, but they are susceptible to time-domain non-idealities and code-dependent output impedance variation [13]–[17].

Outphasing, also known as linear amplification with non-linear components (LINC), is a transmitter architecture that avoids the challenges associated with high amplitude resolution and amplitude-dependent non-linearities, operates in time domain, and is inherently suitable for digital intensive implementation [18]–[28]. The outphasing architecture was first presented by Chireix [18] in 1935 and has gained new interest with the evolution of digital sub-micron CMOS processes, which provide superior time-domain signal processing capabilities that can be utilized in outphasing.

The amplitude modulated RF signal of an outphasing transmitter is formed by summation of two constant-amplitude phase-modulated signals. A digital-intensive phase modulator (PM) can perform the phase modulation with carrier frequency dependent delays, which can be generated with digitally controlled circuits. Additionally, the constant-amplitude signals are not distorted by power amplifier (PA) nonlinearity and can be amplified with efficient switched-mode PAs [29]–[35]. As rail-to-rail signaling can be utilized in the generation and amplification of phase modulated signals, outphasing has potential digitalization and linearity benefits compared to other transmitter architectures which require high resolution RF-DACs and linear PAs.

As will be shown in this paper, wideband discrete-time phase modulators suffer from two architecture-specific sources of adjacent channel leakage ratio (ACLR) degradation. First, the sampling images of the modulating signal are also shifted in frequency by harmonic components of the square-wave carrier and fall on top of the signal band, vastly degrading ACLR. Second, because of discrete-time processing of the modulating phase signal, the phase modulator can generate narrow pulses which are later swallowed in the transmitter chain [36], [37]. As pulse swallowing typically occurs only for one of the phase-modulated signals at a time, the vector sum becomes distorted and transmitter linearity degrades.

Recently, linear interpolation has been suggested in [38] to improve the performance of RF pulse-width modulation (RF-PWM) transmitters [39]. In this paper, the scope has been extended to cover outphasing transmitters with wider relative bandwidth. We have also integrated the concept of linear interpolation into a single digital interpolating phase

Manuscript received MONTH DAY, YEAR; revised MONTH DAY, YEAR. J. Lemberg (e-mail: jerry.lemberg@aalto.fi), M. Kosunen, E. Roverato, M. Martelius, K. Stadius and J. Ryyänen are with the Department of Micro and Nanosciences, School of Electrical Engineering, Aalto University, Espoo, Finland

L. Anttila and Mikko Valkama are with Department of Electronics and Communications Engineering, Tampere University of Technology, Tampere, Finland

This work is supported by Nokia Networks and the Finnish Funding Agency for Technology and Innovation.

Fig. 1. Generic block diagram of an outphasing transmitter.

modulator (DIPM) entity, capable of significantly improving achievable ACLR and EVM. In addition to phase interpolation, the DIPM is shown to address pulse swallowing issues present in digital wideband phase modulators. The DIPM also enables custom carrier frequency generation (CCG) by utilizing only a single frequency reference. With 2.46 GHz sampling rate the carrier can be generated from above DC up to 3 GHz, thus increasing the flexibility of the digital transmitter.

The performance of the DIPM concept is demonstrated with 2.46 GHz RF carrier frequency and 100 MHz OFDM signal, which is one of the working assumptions for the carrier bandwidth of emerging 5G mobile radio networks [40]. With the chosen resolution parameters, the proposed DIPM achieves an ACLR of -59 dBc in outphasing configuration, providing 16 dB improvement when compared to non-interpolating sample-and-hold phase modulator architecture, capable of -43 dBc ACLR with the same simulation parameters.

This paper begins by explaining the operation and challenges of digital phase modulation in Section II. Section III describes the architecture and features of the digital interpolating phase modulator (DIPM). Section IV is dedicated to simulation results, which demonstrate the achievable ACLR of the phase modulator architectures discussed in this paper. The paper ends with conclusions in Section V.

II. OUTPHASING TRANSMITTER OPERATION

A. Outphasing Principle

A generic block diagram of an outphasing transmitter is shown in Fig. 1, where the outphasing presentation of the output signal $V(t)$ can be derived as follows. The amplitude-modulated signal $V(t)$ can be presented in its polar form as

$$V(t) = r(t) \cos(\omega_c t + \phi(t)), \quad (1)$$

where ω_c is the angular carrier frequency and $r(t)$ and $\phi(t)$ correspond to the magnitude and phase of the complex baseband data signal, respectively. In outphasing, the polar form of $V(t)$ is separated into two constant-amplitude outphasing signal components as

$$V(t) = S_1(t) + S_2(t) \quad (2)$$

$$S_{1,2}(t) = \cos(\omega_c t + \Phi_{1,2}(t)), \quad (3)$$

where the modulating signals $\Phi_{1,2}(t)$ consist of the polar phase component $\phi(t)$ and the outphasing angle $\theta(t)$ as

$$\Phi_1(t) = \phi(t) + \theta(t) \quad (4)$$

$$\Phi_2(t) = \phi(t) - \theta(t). \quad (5)$$

The outphasing angle $\theta(t)$ is calculated from the normalized polar vector length $r(t)$ with

$$\theta(t) = \arccos(r(t)), \quad 0 \leq r(t) \leq 1. \quad (6)$$

As depicted in Fig. 1, the phase signals $\Phi_{1,2}(t)$ are derived from baseband complex components I and Q by the signal component separator (SCS). Because of nonlinear signal processing in the signal component separator, the bandwidth of the modulating signal $\Phi(t)$ far exceeds the bandwidth of the original baseband IQ signal [41]. The bandwidth expansion sets further requirements for the sampling rate of a digital system. A general rule of thumb approximation is that ten times the original bandwidth is required to account for the polar vector bandwidth expansion [42]. This indicates that a digital SCS requires a sampling rate in the order of 1 GSample/s to account for the bandwidth expansion of a 100 MHz signal. With the evolution of submicron CMOS processes, implementation of a digital SCS at several GSamples/s [43] is now possible and provides sufficient oversampling for a 100 MHz signal, thus enabling wideband digital phase modulation in outphasing transmitters, capable of replacing conventional D/A-conversion.

B. Operation of the Digital Phase Modulator

As a reference, we first compare our proposed phase modulator architecture to the operation principle of recently implemented digital intensive phase modulators utilized in outphasing transmitters. These outphasing transmitters are capable of clocking the SCS and the phase modulator directly at carrier frequency f_c [24], [25]. In such a system, the phase $\Phi[n]$ is sampled with a sampling rate of $F_s = f_c$.¹ Because the modulating phase remains constant between the sampling instants, we refer to this phase modulator as the sample-and-hold phase modulator (SH-PM).

The phase-modulated square-wave carrier can be expressed as

$$S(t) = \text{sgn}(\cos(\omega_c t + \Phi_{sh}(t))), \quad (7)$$

where $\Phi_{sh}(t)$ is the modulating phase with sample and hold.

Fig. 2 depicts the time-domain operation of SH-PM with both sinusoidal and square-wave carrier. The visible phase jumps in the sinusoidal carrier are a manifestation of abrupt changes in $\Phi_{sh}(t)$.

C. Implementation of the Digital Phase Modulator

The operation principle of the sample-and-hold phase modulator is depicted in Fig. 3(a). The SH-PM can be implemented by delay modulation of the carrier, where delays are proportional to phase values of $\Phi[n]$. Delays can be generated with a digitally controlled delay line (DCDL), and the delay corresponding to $\Phi[n]$ can be then selected with a multiplexer at sampling rate F_s , which generates phase modulation based on $\Phi_{sh}(t)$.

¹A typical requirement for digital transmitters is that the baseband signal must be sampled with integer fraction of the carrier frequency. If the requirement is not met, intermodulation between sampling images and carrier harmonics fill the spectrum with spurious content.

Fig. 2. Time-Domain operation of the SH-PM with sinusoidal and square-wave carriers.

Fig. 3. Block diagram of the SH-PM, presented conceptually in (a) and with a realizable implementation in (b).

An architecture used, e.g., in implementations of [24] and [25] is depicted in Fig. 3(b). The architecture utilizes a segmented strategy to achieve high phase resolution. A multiplexed delay-locked loop (DLL) is used to produce an initial coarse delay, to which an additional fine delay is added with a varactor-based DCDL. The resulting circuit is thus simultaneously capable of achieving high phase resolution and able to perform rapid phase transitions.

D. Sources of Performance Degradation

1) *ACLR Degradation due to Sampling Images:* ACLR degradation in the sample-and-hold phase modulator mainly occurs due to the discrete-time signal processing of $\Phi_{sh}(t)$. This is elaborated in more details below. The Fourier series of 50% duty-cycle square-wave carrier is

$$S_{sq}(t) = \sum_{k=1}^{\infty} \frac{4}{n\pi} \cos(n(\omega_c t)), \quad n = 2k - 1. \quad (8)$$

The carrier is then modulated by the phase signal $\Phi_{sh}(t)$ to produce the output signal $S(t)$ of (7) as

$$S_{msq}(t) = \sum_{k=1}^{\infty} \frac{4}{n\pi} \cos(n(\omega_c t + \Phi_{sh}(t))), \quad (9)$$

indicating that the n th harmonic of the carrier is modulated by $n\Phi_{sh}(t)$.

Fig. 4. The amplitude-modulated signal $V(t)$ of each carrier harmonic, which are based on (9). In the top figure $\omega_c = 0$, and in the bottom figure $\omega_c = 2\pi f_c$. For clarification, the dominant sampling images of each harmonic falling on the carrier are indicated with arrows.

Fig. 5. Harmonic components of the transmitter output signal $V(t)$, which lie near the carrier.

In order to demonstrate the contribution of the sampling images to linearity degradation, the sampled phase $\Phi_{sh}(t)$ of $S_{msq}(t)$ is divided to the baseband component $\Phi_0(t)$ and the sampling image components $\Phi_i(t)$ as

$$\begin{aligned} S_{sh}(t, n) &= \frac{4}{n\pi} \cos \left(n \left(\omega_c t + \Phi_0(t) + \sum_i \Phi_i(t) \right) \right) \quad (10) \\ &= \frac{4}{n\pi} \cos(n\omega_c t) \cos \left(n\Phi_0(t) + n \sum_i \Phi_i(t) \right) \\ &\quad - \frac{4}{n\pi} \sin(n\omega_c t) \sin \left(n\Phi_0(t) + n \sum_i \Phi_i(t) \right). \end{aligned}$$

Because the terms

$$\cos \left(n\Phi_0(t) + n \sum_i \Phi_i(t) \right) \text{ and } \sin \left(n\Phi_0(t) + n \sum_i \Phi_i(t) \right)$$

have images at multiples of the sampling frequency F_s , they are frequency shifted with $\cos(n\omega_c t)$ and $\sin(n\omega_c t)$ to fall on top of the fundamental signal at the carrier frequency f_c , if F_s is an integer fraction of f_c . This is graphically illustrated in Fig. 4, where the n th harmonic is derived from

$$V(t, n) = S_{sh1}(t, n) + S_{sh2}(t, n) \quad (11)$$

Fig. 4 depicts the signal spectra up to the 7th harmonic of $V(t, n)$, in cases with $\omega_c = 0$ and $\omega_c = 2\pi f_c$. In the case of $\omega_c = 0$, it can be seen that the behavior of the fundamental and the harmonics is different due to the multiplication in $n\Phi_{sh}(t)$. When $\omega_c = 2\pi f_c$, it is evident that the sampling images fall on the carrier after modulation by the harmonic frequency components.

A close-up of the sampling images on top of the carrier is depicted in Fig. 5. Each image, modulated by a higher harmonic component of the carrier, is attenuated more than the lower orders due to the sinc frequency response of the sample and hold operation, as well as the amplitude scaling in the harmonic components.

It can be noted from (10) that removing the sampling images leads to the desired phase-modulated signal presented in (3), which can be shown with

$$\lim_{\sum \Phi_i \rightarrow 0} S_{sh}(t, n) = \cos(n(\omega_c t + \Phi_0(t))). \quad (12)$$

This directly indicates that the ACLR can be improved by further attenuating the sampling images $\Phi_i(t)$.

To summarize the previous analysis, the sinc filtering provided by sample-and-hold based phase processing insufficiently attenuates the sampling images $\Phi_i(t)$, which degrade the ACLR as they fall on the carrier due to harmonic frequency shift. In theory, the most straightforward method to improve ACLR is to increase oversampling $\frac{F_s}{f_c}$ to remove the images at the frequencies shifted onto the signal band by the dominating carrier harmonic components. It is later in this paper demonstrated that only a moderate ACLR improvement can be achieved with an additional 4x oversampling, at $4 \times F_s \approx 10\text{GHz}$ sampling rate, which is unfeasible with existing CMOS processes. However, digital interpolation can be performed to the modulating phase signal $\Phi[n]$ to improve ACLR, as was suggested in [38]. The digital interpolation further attenuates the sampling images without the need for additional oversampling.

2) *ACLR Degradation due to Pulse Swallowing*: As presented in Fig. 2, the sample-and-hold phase modulator creates narrow pulses due to the rapid phase transitions inherent to the architecture. A narrow pulse is generated whenever

$$\Phi[n] \leq \frac{\pi}{2} \leq \Phi[n-1] \quad (13)$$

$$\Phi[n] \leq \frac{3\pi}{2} \leq \Phi[n-1]. \quad (14)$$

In such a scenario, the sign of $S(t)$ at the end of the sampling period is inverted at the beginning of the next period. The occurrence of a narrow pulse does not inherently degrade outphasing transmitter linearity. The degradation emerges only if the circuit cannot reproduce the pulse due to its narrow width, resulting to the pulse being swallowed inside the transmitter chain. Due to the phase difference created by the outphasing angle $\theta(t)$, pulse swallowing often occurs only in $S_1(t)$ or $S_2(t)$ at a time. Thus, pulse swallowing generates distortion to the output waveform $V(t)$.

A time-domain demonstration of pulse swallowing is shown in Fig. 6, where the pulse-swallowed (grey) waveform of the modulated carrier $V(t)$ differs from the ideal waveform

Fig. 6. Time-Domain occurrence of pulse-swallowing. The sum of ideal signals (black), differs from the sum with swallowed pulses (grey). Therefore pulse swallowing leads to linearity degradation.

(black). The severity of pulse swallowing is dependent on the maximum pulse width that is swallowed in the transmitter chain. The ACLR degradation due to pulse swallowing with SH-PM is further analyzed and illustrated with simulations in Section IV.

III. PROPOSED DIGITAL INTERPOLATING PHASE MODULATOR (DIPM)

The sample-and-hold phase modulator described in Section II provides means to digitally control the phase of the carrier with fine resolution and a feasible sampling rate. Instead of sample-and-hold, it is possible to apply linear interpolation to improve the approximation of the instantaneous phase between the sampling instances of $\Phi[n]$. Linear interpolation further attenuates the sampling images of the modulating phase signal with the sinc^2 frequency response, which is shown in Section IV to significantly improve ACLR.

With a sinusoidal signal, precise knowledge of the instantaneous phase is required in order to reconstruct the continuous waveform of the modulated carrier. However, in the case of a square-wave signal it is sufficient to only locate the zero crossings of the modulated carrier to reconstruct the signal at the modulator output. This feature is exploited in the proposed phase modulator to implement linear interpolation without increasing the sampling rate.

A. Estimation of Zero Crossings with Digital Interpolation

In order to determine the zero crossings of the phase modulated signals, we begin by defining the continuous phase signal as

$$\rho_{1,2}(t) = \omega_c t + \Phi_{1,2}(t), \quad (15)$$

where $\Phi_{1,2}(t)$ are the modulating phase signals according to (3). The discrete-time presentation of $\rho_{1,2}(t)$ can be more generally expressed as

$$\rho[n] = \alpha + \Phi[n], \quad (16)$$

where α signifies the constant phase increment, defined by the carrier frequency f_c and sampling rate F_s as

$$\alpha = 2\pi \frac{f_c}{F_s}. \quad (17)$$

Thus, in the case of $F_s = f_c$, as assumed in this paper, $\alpha = 2\pi$. To perform linear interpolation, the discrete-time

phase difference is obtained as

$$\Delta\rho[n] = \alpha + \Phi[n] - \Phi[n-1]. \quad (18)$$

Thus, the interpolated phase value at fractional time increment k after $n-1$ is

$$\rho_{int}[n, k] = \rho[n-1] + \frac{k}{K} \cdot \Delta\rho[n], \quad k = 1, \dots, K, \quad (19)$$

where K determines the number of fractions the sampling period is divided into, and k indicates the position between sampling instants n and $n-1$.

The idea behind determining the zero crossing is illustrated in Fig. 7. The zero crossings of the phase-modulated carrier $S(t)$, are determined by

$$S[n, k] = \cos(\rho[n, k]) = 0, \quad (20)$$

where $\rho_{int}(n, k)$ are the corresponding phases of the outphasing signals in discrete time representation. The zero crossings X_i can be solved from

$$\rho_{int}[n, X_i] = \left(\frac{1}{2} + i\right) \pi, \quad i = 0, 1, 2, \dots, \quad (21)$$

where X_i represents the value of k closest to the zero crossing.

To perform the computation of the zero crossing the following aspects must be taken into account. Because of finite wordlength used to present the 2π phase range, the phase signal is wrapped as

$$\rho[n] = (\alpha n + \phi[n] \pm \theta[n]) \bmod 2\pi, \quad (22)$$

presenting the phase of the output signal at the sampling instant. To compute $\Delta\rho[n]$ correctly, $\phi[n]$ must be unwrapped to prevent errors due to overflows, when the 2π boundary is exceeded.² This results in

$$\Delta\rho[n] = \alpha + \Delta\phi_{uw}[n] \pm \Delta\theta[n], \quad (23)$$

where

$$\Delta\phi_{uw}[n] = \begin{cases} \Delta\phi[n], & |\Delta\phi[n]| \leq \pi \\ \Delta\phi[n] - 2\pi, & \Delta\phi[n] > \pi \\ \Delta\phi[n] + 2\pi, & \Delta\phi[n] < -\pi, \end{cases} \quad (24)$$

$$\Delta\phi[n] = \phi[n] - \phi[n-1], \quad (25)$$

$$\Delta\theta[n] = \theta[n] - \theta[n-1]. \quad (26)$$

The time-domain behavior of the phase-modulated carrier can then be observed from

$$S_{int}[n, k] = \cos(\rho_{int}[n, k]). \quad (27)$$

Fig. 8 depicts the difference in the case of a continuous sinusoidal carrier with SH-PM and DIPM, demonstrating the absence of discontinuities.

Magnitude limits of the phase increment in (23) can be used to obtain insight of time-domain behavior of the DIPM. The maximum phase difference of the polar phase $\Delta\phi[n]$ is $\pm\pi$, due to phase unwrapping. The maximum difference of the outphasing angle $\Delta\theta[n]$ is $\pm\frac{\pi}{2}$, which is the range where $\theta[n]$

²In hardware implementations the phase unwrapping is performed inherently by two's complement arithmetic.

Fig. 7. Graphical illustration of the linear solver for zero-crossings.

Fig. 8. Time-domain behavior with a sinusoidal carrier of SH-PM and DIPM shown side by side.

is defined. Thus, the maximum difference of the modulating phase signal can be defined as

$$\Delta\Phi_{max} = \Delta\phi_{max} + \Delta\theta_{max} = \pi + 0.5\pi = 1.5\pi. \quad (28)$$

If clocked at $F_s = f_c$, the maximum and minimum phase difference of the phase modulated carrier can be determined as

$$\Delta\rho_{max} = \alpha + \Delta\Phi_{max} = 2\pi + 1.5\pi = 3.5\pi \quad (29)$$

$$\Delta\rho_{min} = \alpha - \Delta\Phi_{max} = 2\pi - 1.5\pi = 0.5\pi. \quad (30)$$

Based on (29) and (30), the DIPM must be able to produce at maximum four sign changes during a sampling period. The minimum phase difference of 0.5π defines that the DIPM must be capable of only producing one sign change in two sampling periods.

The linear interpolation of the phase signal leads to a well defined time-domain behavior for the DIPM. The shortest pulse which the DIPM generates is dictated by a phase shift of π at the maximum phase increment $\Delta\rho_{max} = 3.5\pi$ as

$$T_{min} = \frac{1}{3.5f_c} = 0.29T_c. \quad (31)$$

Thus, the architecture of the DIPM guarantees that for example at the carrier frequency $f_c = 2.46$ GHz, the minimum pulse width is limited to approximately 115 ps.

B. Custom Carrier Generation (CCG)

Let us assume that the sinc^2 response of linear interpolation is capable of attenuating the sampling images of $S_{int}(t)$ below quantization noise. In such a scenario, the sampling images no longer affect the ACLR even if the carrier frequency is altered while retaining constant sampling rate. Therefore, we now consider the possibility that the DIPM can generate a wide range of carrier frequencies with a single sampling rate, without affecting the properties of the modulating signal.

The carrier frequency in the DIPM is determined by the constant value of α , which in the case of $F_s = f_c$ is 2π . As the value of the parameter α solely determines the carrier frequency, we can consider it as a variable. A valid range definition for the variable α is then required. The range can be derived from the minimum requirements we have already set on the phase modulator. It was defined earlier that the DIPM must support four sign changes during a sampling period, which corresponds to a phase difference of 4π . On the other hand, the maximum phase difference was defined in (29) to be 3.5π , which suggests that α can be as high as 2.5π without any overflows in the phase calculation. The DIPM is thus guaranteed to function correctly up to the carrier frequency of

$$f_{c_{max}} = \frac{2.5}{2} F_s = 1.25 F_s. \quad (32)$$

The carrier frequency of the DIPM can be calculated with the following formula

$$\alpha = \frac{f_c}{F_s} 2\pi, \quad f_c = \left[0, \frac{2.5}{2} F_s \right], \quad (33)$$

where F_s is the system sampling rate and f_c is the parametrized carrier frequency. The DSP internal resolution defines the resolution of f_c , unconstrained by the phase resolution of the modulator. However, very low carrier frequencies are unfeasible because the modulated harmonic components of the square-wave carrier will overlap with the fundamental component.

Based on (32), with $F_s = 2.46$ GHz and maximum of four sign transitions during a carrier period, the DIPM is capable of generating the carrier frequency from DC up to 3 GHz. According to earlier analysis, the number of output transitions per sampling period limit the maximum carrier generation frequency $f_{c_{max}}$. To further increase $f_{c_{max}}$, the capability to perform more output transitions during the sampling period could be added.

C. Implementation

The entity of the digital interpolating phase modulator (DIPM) can be constructed from a DSP unit and an RF front end, as depicted in Fig. 9. In the case of a constant-amplitude phase-modulated square-wave signal, as with outphasing signals S_1 and S_2 , the information is coded into the moments when the square-wave signal changes polarity. The DIPM uses this property with linear interpolation to generate high time resolution phase modulation. Thus, the DSP unit performs linear interpolation and calculates the instantaneous phase of the modulated carrier, from which it locates the time instances

when the modulated RF signal has a zero crossing and changes polarity. The task of the RF front end is to change the sign of the output signal with delays defined by the DSP unit. Based on (29), the DIPM can produce a maximum of four zero crossings during one sampling period. Therefore, the DIPM is divided into four sub-units, each capable of generating a change in polarity and operating only for one fourth of the sampling period. The outputs of the four units are combined into a single high-and-low toggling output, which reconstructs the modulated square-wave carrier $S(t)$.

1) *DSP Unit*: The task of the DSP unit is to solve (21), which involves

- performing linear interpolation between the incoming phase samples, and
- finding the zero-crossings of the phase-modulated output signal.

Fig. 9 depicts an example implementation of the DSP unit. The incoming phase signal $\rho[n]$ is sampled at F_s , and the wordlength is determined by the desired phase resolution. Because each sampling period can have up to four zero crossings, (21) is first split into four linear sub-equations. Each sub-equation corresponds to a quarter of the n th sampling period, and has the form

$$A_i + B \cdot \frac{k}{K/4} = \{0, \pm\pi\}, \quad i = 0, \dots, 3, \quad (34)$$

where A_i represents the partial initial phase, B the partial phase increment, and k is the time at which a possible zero crossing occurs. Here, A_i is calculated for each quarter period as

$$A_i = \rho[n-1] + i \cdot \frac{\Delta\rho[n]}{4}, \quad (35)$$

while B is given by

$$B = \frac{\Delta\rho[n]}{4}. \quad (36)$$

The solution can then be found for example through the binary search algorithm [44], which can be pipelined for high-speed digital implementation. The number of stages in the binary search algorithm is equal to the resolution of k , which is one fourth of the overall phase resolution K . The binary search algorithm can thus be implemented with sufficiently high resolution not to degrade transmitter performance. If no zero crossing is found, the enable signal e_i is de-asserted, meaning that no sign change will take place in that fraction of the sampling period.

2) *RF Front End*: The DIPM requires an RF front end to perform digital-to-time conversion (DTC) for the zero crossings which occur in the modulated carrier.

The requirements set for the front end are as follows:

- The DSP unit controls four parallel digital-to-time converters (DTC), which together generate the modulated carrier signal.
- Each DTC can change the state of the output of the DIPM in its own quarter of the sampling period.
- It is possible that no zero crossings occur inside the DTC. Thus, the DTC and the modulator output must be able to maintain their state when required.

Fig. 9. Block diagram of the proposed DIPM, with details of the DSP unit and the RF front end. The DSP unit divides the interpolation into four solvers, which control digital-to-time converters inside the RF front end. The pulses generated by DTCs are combined in the output stage which toggles the sign of the modulator output.

The proposed solution for the RF front end is shown in Fig. 9, where each DTC consists of delay generation controlled by $k_i[n]$, enable functionality via $e_i[n]$ and a pulse generator. The pulses from each DTC are combined in an OR gate into a signal $T(t)$, which toggles a T flip-flop to reconstruct the phase-modulated square-wave carrier $S(t)$.

Delay generation of the proposed architecture is modified from [25], [26], and consists of a coarse delay generated with a DLL operating at F_s . The DLL is cascaded with a varactor-based DCDL capable of generating a fine incremental delay. The DLL enables convenient division of the sampling period into four sections, whereas the DCDL is employed to increase the phase resolution of a single DTC to $N-2$ bits, such that the total phase resolution of the DIPM reaches N bits. The enable bit multiplexes between the DLL output and the ground voltage, preventing the occurrence of rising edges when needed. Due to the fact that the DLL and DCDL are sensitive to PVT variations, extensive calibration and predistortion, also employed in [26], may be required to achieve desired effective phase resolution.

An additional rising edge impulse generator is utilized to shorten the pulse widths clearly below one fourth of the sampling period after the DLL and DCDL. The pulse generator guarantees that the signals do not overlap in the OR-Gate, and that all of the triggering pulses reach the T flip-flop. Thus, the pulse generator makes it possible to utilize a 50% duty cycle in the DLL and DCDL.

IV. PERFORMANCE EVALUATION BY SIMULATIONS

A. Transmitter Characteristics

The simulations in this paper were performed with the following parameters, unless otherwise stated:

- The baseband signal has 100 MHz bandwidth (BW) and consists of five aggregated 20 MHz 64-QAM OFDM carriers, with a peak to average power ratio (PAPR) of 12 dB.
- The SCS and the phase modulator are clocked at the carrier frequency, such that $F_s = f_c = 2.46$ GHz.

- The phase modulator resolution is 10 bits, and thus the sampling period is quantized into $K = 2^{10} = 1024$ steps with a delay resolution of approximately 400 fs.

A sufficiently high baseband signal oversampling rate of $\frac{F_s}{BW} \approx 25$ has been chosen to avoid performance issues caused by bandwidth expansion. A delay resolution of 400 fs is achievable with proper calibration of a digitally controlled delay line [45], while generating low enough quantization noise to detect the sampling images near the carrier.

B. SH-PM Performance

In these simulations we compare the outphasing transmitter ACLR and overall spectral performance of the two presented phase modulator architectures. The ACLR of the DIPM is compared against the SH-PM, which is first simulated in detail.

1) *ACLR Degradation due to Sampling Images*: The linearity of the SH-PM degrades due to the square-wave carrier harmonic frequency shift, if the baseband signal has insufficiently attenuated sampling images. The sampling images from harmonics shift on top of the carrier, degrading the ACLR.

The ACLR degradation is verified and illustrated in Fig. 10, where an outphasing transmitter utilizing SH-PMs with both sinusoidal and square-wave carriers are simulated. Using a sinusoidal carrier without harmonic components results in the ACLR of -60 dBc. With a square-wave carrier, the ACLR degrades to -43 dBc, with a similar envelope of the spectrum as in Fig. 4. The ACLR simulation results for the SH-PM with a square-wave carrier are depicted in Fig. 11.

In order to demonstrate the moderate improvements achieved by oversampling the phase signal to a multiple of the carrier frequency, a simulation with 4x baseband oversampling was performed. The results are presented in Fig. 12, where the spectra are shown for both sinusoidal and square-wave carriers. Although the image content degrading the ACLR is less obtrusive, with an ACLR of -48 dBc, the degradation caused by the sampling images is still visible well above the quantization noise. Moreover, the 4x oversampling would require the DSP to operate at approximately 10 GHz in the

Fig. 10. The spectra of sinusoidal and square-wave modulated carriers in an outphasing transmitter with 10-bit SH-PMs.

Fig. 12. The spectra of sinusoidal and square-wave carriers modulated with 4x oversampled baseband-data.

Fig. 11. The ACLR1 measurement of the SH-PM gives -43 dBc, but degrades to -41 dBc at ACLR2.

Fig. 13. Spectra of the SH-PM with different pulse-swallowing thresholds. With a 100 ps threshold the ACLR1 further degrades by 4 dB from ideal -43 to -39 dBc.

case of a 2.46 GHz carrier frequency, which is currently unfeasible even with most advanced CMOS processes..

2) *ACLR Degradation due to Pulse Swallowing*: The maximum operation frequency of the transmitter blocks limit the pulse width propagating inside the transmitter chain. Too narrow pulses will be swallowed when they propagate through the circuit. For a single inverter in a modern CMOS process the pulse swallowing threshold can be approximated to be in the order of 20 ps, whereas for a switched-mode PA the threshold can be well over 100 ps.

The effect of pulse swallowing on the SH-PM based transmitter ACLR can be estimated by defining a threshold for the simulator, which swallows all pulses with smaller width than specified. The simulation results are shown in Fig. 13 with the spectra and corresponding ACLRs. The simulations indicate that the ACLR degradation is relative to the pulse swallow threshold.

C. Digital Interpolating Phase Modulator (DIPM)

1) *Improved ACLR due to Sampling Image Suppression*: The linear interpolation performed by the DIPM improves approximation of the instantaneous phase, such that the sampling images of the modulating signal are further attenuated than with the SH-PM.

In Fig. 14 the spectra of the SH-PM and the DIPM are compared. The ACLR of the DIPM is -59 dBc, which is close

to the result of the sinusoidal carrier SH-PM of -60 dBc in Fig. 10. The result indicates that the sampling images of the modulating signal are sufficiently attenuated in the proposed DIPM not to significantly affect ACLR. The corresponding ACLR simulation for the DIPM with a square-wave carrier is presented in Fig. 15.

The DIPM effectively attenuates the sampling images, thus improving not only the ACLR, but also the error vector magnitude (EVM) by increasing the in-band signal to noise ratio. The EVM measurement for the SH-PM and the DIPM is depicted in Fig. 16, where the DIPM produces similar EVM results for each component carrier, in contrast to the SH-PM which degrades the EVM on carriers further away from the center frequency. This behavior can be explained with the sinc filtering of the sampling images which are frequency shifted on top of the signal band. However, the EVM results for both phase modulators are more than sufficient to meet e.g. the 3GPP standard EVM specification of 8% for 64-QAM [46].

2) *ACLR Degradation due to Pulse Swallowing*: The DIPM virtually prevents pulse swallowing with a minimum pulse width of 115 ps when $f_c = 2.46$ GHz, as in (31). Further analysis on the probabilistic behavior of pulse swallowing is beyond the scope of this paper.

3) *Custom Carrier Generation (CCG)*: Custom carrier generation is possible due to the phase interpolation performed in

Fig. 14. The figure presents the spectral behavior of the SH-PM and the DIPM based outphasing transmitters with a square-wave carrier. The linear interpolation utilized in the DIPM is capable of improving the ACLR by 16 dB.

Fig. 15. The ACLR1 measurement of the DIPM gives -59 dBc, and improves to -60 dBc at ACLR2.

the DIPM. The constant phase increment provided by α of (33) defines the carrier frequency in respect to the system sampling frequency F_s .

Custom carrier generation was simulated with several carrier frequencies to validate the concept. The simulated spectra are shown in Fig. 17. The simulation was first performed with $f_c = F_s = 2.46$ GHz, and the carrier frequency was then altered to 2 GHz, 1.5 GHz and finally to 1 GHz. The ACLR remains unaffected in all simulations, demonstrating the functionality of the CCG concept. However, setting the carrier frequency far below 1 GHz with the 100 MHz baseband bandwidth leads to a situation where ACLR begins to degrade as the wide square-wave carrier third harmonic begins to overlap with the signal band. In the case of a sub-gigahertz carrier frequency, the ratio of the baseband signal bandwidth to the carrier frequency should thus be carefully considered.

V. CONCLUSION

In this paper, we have presented a new phase modulator architecture for outphasing transmitters. The proposed digital interpolating phase modulator (DIPM) was demonstrated to provide additional filtering to the sampling images of the phase signal. The linear phase interpolation performed by the DIPM practically eliminates ACLR degradation caused by modulation between sampling images and carrier harmonics,

Fig. 16. EVM measurements for the five aggregated 64-QAM 20MHz component carriers with the SH-PM and the DIPM. The left figure depicts EVM for each individual carrier, and the right figure shows the EVM constellation for all carriers. The EVM of the SH-PM carriers degrade further away from the center frequency due to the interfering noise from the insufficiently attenuated sampling images.

Fig. 17. Custom Carrier Generation with DIPM. The carrier frequency is generated through (33) at frequencies 2.46 GHz, 2 GHz, 1.5 GHz and 1 GHz.

which is visible in the sample-and-hold phase modulator architecture.

The DIPM-based outphasing transmitter achieves an ACLR of -59 dBc with a 100 MHz OFDM baseband signal, when simulated with 10-bit phase modulators at a sampling rate of 2.46 GHz. Thus, the DIPM is capable of improving ACLR by 16 dB when compared to a more conventional sample-and-hold phase modulator architecture, which achieves -43 dBc ACLR with similar resolution and design parameters.

The DIPM also enables the use of custom carrier generation, which makes generation of a nearly arbitrary carrier frequency below the system sampling rate possible. As custom carrier generation does not affect the ACLR characteristics of the proposed phase modulator, the carrier can be generated to a wide frequency range while utilizing only a single frequency reference. This in turn simplifies digital-intensive system-on-chip transmitter design.

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Jerry Lemberg was born in Lohja, Finland, in 1986. He received his Master of Science degree in electrical engineering from Aalto University, Espoo, Finland, in 2013. He is currently working towards the Doctoral degree as a research scientist at the School of Electrical Engineering, Aalto University. His research interests include high-speed digital-to-analog converters and digital intensive transmitters.

Marko Kosunen (S'97-M'07) received his M.Sc., L.Sc. and D.Sc. (with honors) degrees from Helsinki University of Technology, Espoo, Finland, in 1998, 2001 and 2006, respectively. He is currently a Senior Researcher at Aalto University, Department of Micro and Nanosciences. His expertise is in implementation of the wireless transceiver DSP algorithms and communication circuits. He is currently working on implementations of cognitive radio spectrum sensors, digital intensive transceiver circuits and medical sensor electronics.

Enrico Roverato (S'13) was born in Padova, Italy, in 1988. He received the B.Sc. degree in information engineering from University of Padova, in 2010, and the M.Sc. degree in electrical engineering from Aalto University, Espoo, Finland, in 2012. He is currently a researcher at Aalto University, Department of Micro- and Nanosciences, where he is working towards the Ph.D. degree. His research interests are on all-digital RF transmitter circuits, with special focus on the implementation of high-speed DSP algorithms.

Mikko Martelius was born in Laitila, Finland, in 1988. He received his Master of Science degree in electrical engineering from Aalto University, Espoo, Finland, in 2015. He is currently working towards the Doctoral degree at Aalto University, Department of Micro- and Nanosciences. His research interests include switch-mode power amplifiers and digital intensive transmitters.

Kari Stadius (S'95-M'03) received the M.Sc., Lic. Tech., and Doctor of Science degrees in electrical engineering from the Helsinki University of Technology, Helsinki, Finland, in 1994, 1997, and 2010, respectively. He is currently working as a staff scientist at the Department of Micro- and Nanosciences, Aalto University School of Electrical Engineering. His research interests include the design and analysis of RF transceiver blocks with special emphasis on frequency synthesis. He has authored or coauthored over 70 refereed journal and conference papers in the areas of analog and RF circuit design.

Lauri Anttila Lauri Anttila (S'06, M'11) received the M.Sc. degree and D.Sc. (Tech) degree (with honors) in electrical engineering from Tampere University of Technology (TUT), Tampere, Finland, in 2004 and 2011. Currently, he is a postdoctoral research fellow at the Department of Electronics and Communications Engineering at TUT. He has published over 50 articles in international peer-reviewed journals and conferences, as well as two book chapters. His research interests include signal processing for wireless communications, digital front-end signal processing, transmitter and receiver linearization, power-efficient transmitter structures, and radio implementation challenges in 5G cellular radio and full-duplex radio.

Mikko Valkama Mikko Valkama was born in Pirkkala, Finland, on November 27, 1975. He received the M.Sc. and Ph.D. Degrees (both with honors) in electrical engineering (EE) from Tampere University of Technology (TUT), Finland, in 2000 and 2001, respectively. In 2002, he received the Best Ph.D. Thesis -award by the Finnish Academy of Science and Letters for his dissertation entitled "Advanced I/Q signal processing for wideband receivers: Models and algorithms". In 2003, he was working as a visiting researcher with the Communications Systems and Signal Processing Institute at SDSU, San Diego, CA. Currently, he is a Full Professor and Department Vice-Head at the Department of Electronics and Communications Engineering at TUT, Finland. His general research interests include communications signal processing, estimation and detection techniques, signal processing algorithms for software defined flexible radios, cognitive radio, full-duplex radio, radio localization, 5G mobile cellular radio, digital transmission techniques such as different variants of multicarrier modulation methods and OFDM, and radio resource management for ad-hoc and mobile networks.

Jussi Ryyänen (S'99-M'04) was born in Ilmajoki, Finland, in 1973. He received his Master of Science, Licentiate of Science, and Doctor of Science degrees in electrical engineering from Helsinki University of Technology (HUT), Helsinki, Finland, in 1998, 2001, and 2004, respectively. He is currently working as an associate professor at the Department of Micro- and Nanosciences, Aalto University School of Electrical Engineering. His main research interests are integrated transceiver circuits for wireless applications. He has authored or coauthored over 100 refereed journal and conference papers in the areas of analog and RF circuit design. He holds six patents on RF circuits.