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Silicon-based Coulomb blockade thermometer with Schottky barriers

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A hybrid Coulomb blockade thermometer (CBT) in form of an array of intermittent aluminum and silicon islands connected in series via tunnel junctions was fabricated on a thin silicon-on-insulator (SOI) film. Tunnel barriers in the micrometer size junctions were formed by metal-semiconductor Schottky contacts between aluminium electrodes and heavily doped silicon. Differential conductance through the array vs. bias voltage was found to exhibit characteristic features of competing thermal and charging effects enabling absolute temperature measurements over the range of ~65 to ~500 mK. The CBT performance implying the primary nature of the thermometer demonstrated for rather trivial architecture attempted in this work paves a route for introduction of Coulomb blockade thermometer into well-developed contemporary SOI technology. © 2014 AIP Publishing LLC.

Tunnel junctions are frequently employed as elemental building blocks in fabrication of micro- and nano-devices which operation is based on the single electron tunneling phenomena.¹ One of the numerous applications enabled by single electron devices is in the field of absolute thermometry for cryogenic temperatures, especially in the sub-Kelvin range. The great advantage is that an absolute thermometer measures temperature directly without any need for additional calibration against a reference thermometer. Since in absolute thermometry voltages and currents are directly related to the temperature, with proportionality coefficients being just universal physical constants, development of temperature scale standards becomes more straightforward. In particular, this is of high relevance for the temperature range below 500 mK where, at present, there are no widely accepted standards for reliable temperature scale calibration. Different approaches involving single charge processes have been suggested mainly based on the assessment of temperature dependence of shot-noise,² Coulomb blockade and electron tunneling through a single junction.³,⁴

The concept of Coulomb blockade thermometer (CBT) is based on the temperature dependent partial Coulomb blockade in a single-electron tunneling. Typical device is formed by an array of micrometer size tunnel junctions between normal electrodes connected in series. Electrical conductance due to charge tunneling through the array shows temperature dependence provided that the CBT operates in a weak Coulomb blockade regime, i.e., its charging energy $E_c \approx k_BT$. Charging energy of $N$ tunnel junctions connected in series is $E_c = [(N-1)/N]e^2/C_\Sigma$, where $C_\Sigma$ is total capacitance of an island (electrode) between the junctions in the array. Then, the differential conductance $G$ normalized to its asymptotic value $G_T$ at high bias voltages $V_{bias}$ was shown to follow:³,⁴

$$G(V)/G_T = 1 - (E_c/k_BT)g(eV/Nk_BT), \quad (1)$$

where $g(x) = [x \sinh(x) - 4 \sinh^2(x/2)]/[8 \sinh^4(x/2)]$.

For primary thermometry, temperature is derived from experimentally measured full width at half minimum $V_{1/2}$ of the conductance dip Eq. (1):

$$V_{1/2} \approx 5.439Nk_BT/e. \quad (2)$$

As it follows from Eq. (1), there is no dependence on the particular geometry of the electrodes or the material the thermometer is made of.

Alternatively, CBT thermometer can be used in a secondary mode, viz., temperature is related to the depth of the zero-biased conductance dip $\Delta G = G_T - G(V_{bias} = 0)$ by the following equation written in the lowest order in $E_c/k_BT$:⁵

$$\Delta G/G_T \approx E_c/6k_BT. \quad (3)$$

Recently, it was shown that CBT operation range of temperatures can be extended into the intermediate Coulomb blockade regime where $E_c \sim k_BT$ (i.e., to lower temperatures) by adding higher order terms in Eqs. (2) and (3):⁶

$$V_{1/2} \approx 5.439Nk_BT(1 + 0.3921\Delta G/G_T)/e, \quad (4)$$

$$\Delta G/G_T \approx 1/6(E_c/k_BT) - 1/60(E_c/k_BT)^2$$

$$+ 1/630(E_c/k_BT)^3. \quad (5)$$

In CBT demonstrated so far tunnel junctions were formed between all-metallic electrodes. Aluminum is the most widespread material employed for fabrication of high quality insulating barriers in the junctions. A uniform and free of pinholes dielectric layer of native oxide (≤2 nm) can be easily grown by in-situ fixation. Despite of the advantages, there are also well known drawbacks limiting application of aluminum tunneling structures to mainly basic

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research in academic laboratories, e.g., characteristics of an aluminum oxide barrier is well known to change with time leading to poor long-term stability, uncontrolled drift of parameters, and even loss of the desired functionality. There are also serious difficulties in fabrication of homogeneous large area tunnel junctions (tens and hundreds of square micrometers). Aiming at technologically feasible applications and solutions implementing Coulomb blockade in charge tunneling, devices produced using silicon as a basic material and exhibiting the desired functionality would be of great interest for future transfer to modern silicon technology complying with the determinant paradigms of large scale integration and mass-production. Metal-semiconductor junctions with Schottky barriers have many advantages in this respect exhibiting much better long-term stability, reproducibility, fabrication yield, being also less vulnerable to electrostatic discharge as compared to all-metal tunnel junctions with aluminum oxide barriers. Besides, tunneling transport characteristics can be tuned to certain extend via control over the physics and chemistry of the Schottky barrier. Metal-semiconductor tunnel junctions have been utilized in low-temperature microcoolers for effective electronic cooling down to 40 mK through hot quasiparticle tunneling. So far, there have been no attempts to extend use of Schottky junctions to other types of low temperature tunneling devices. In the present Letter, we report on a CBT sensor with Schottky barrier tunnel junctions fabricated on a heavily doped silicon-on-insulator (SOI) film.

Figure 1 shows the CBT structure with a schematic diagram of the measurement setup. An array of 100 metal-semiconductor tunnel junctions connected in series with total resistance of 321 kΩ was formed by small area contacts (~1.4–1.7 μm²) between overlapping Al and n-type Si islands. The Si islands were fabricated from the active device layer of a SOI wafer heavily doped with As. The thickness of the device layer was 180 nm and the resistivity was ~1 mΩ cm; buried oxide and the handle Si (20 Ω cm) were 400 nm and 500 μm thick, respectively. Both Al and Si electrodes ~10 x 30 μm in size were patterned by standard photolithography. First, Si mesa (bottom electrodes in Fig. 1) was patterned and etched by Reactive Ion Etching in SF₆ plasma. Then, ~550 nm of Al was deposited by sputter deposition; top electrodes were patterned and chemically etched in a phosphoric acid etchant. After etching, Al was sintered by annealing in the forming gas at 410°C for 10 min.

Electrical characterization of the fabricated CBT device was performed in a dry ³He/⁴He dilution refrigerator enabling measurements at variable temperatures down to as low as 12 mK. The device under test (DUT) was mounted on a sample stage which temperature (referred further as a bath temperature T) was measured independently by two sensors of the nuclear orientation thermometer (⁶⁰Co). Since for operation the CBT electrodes are supposed to be in the normal state at the temperatures of interest, a permanent magnet was attached to the sample holder in close proximity to the DUT in order to suppress superconductivity in the Al electrodes. The heavily doped Si in the SOI was tested to retain its normal state at all temperatures down to terminal 12 mK even without the external magnetic field. Differential conductance through the CBT array G was measured as a function of bias voltage V at different temperatures. For this purpose, small amplitude modulation sinusoidal signal V_{mod} was mixed to the bias V = V_{gen} R_2/(R_1 + R_2), while slowly sweeping the generator voltage V_{gen} (see Fig. 1). Minimizing the influence of the modulation signal, V_{mod} was always less than 2% of the full width at half maximum V_{1/2} of the conductance dip (Eq. (1)). This ensured that the shape of the dip was not affected by the injected modulation current. The differential conductance was derived from the measurements of small current δI and voltage δV signals caused by the modulation using the lock-in technique and low-noise current and voltage preamplifiers.

The differential conductance vs. bias is presented in Fig. 2 for different bath temperatures. At the selected temperatures, the conductance was found to exhibit a distinctive dip at bias voltages around zero caused by the Coulomb blockade in the single-electron tunneling through the CBT array due to the finite charging energy.

Both the width of the dip and the value of the conductance at zero bias are seen to vary with temperature. Figure 2(b) shows, for example, a selected conductance dip for 206 mK with a theoretical curve fitted using Eq. (1). The charging energy E_C/k_B ≈ 50 mK required for the fitting was derived from Eq. (5) applied to the conductance measurements at higher temperatures at which thermal gradient
between the CBT device and the cold stage was believed to be negligible. Therefore, the CBT temperature was assumed to be the same as that of the bath measured by the calibrated thermometers mounted on the cold stage. Both the depth of the experimental dip in Fig. 2(b) and its width at half minimum are seen to be in agreement with calculated values of ~0.96 and ~9.7 mV, respectively. Despite of this, the theoretical curve is seen to deviate noticeably from the experimental dip measured at 206 mK.

The electrons in the CBT islands are thermalized via electron-phonon coupling and thermal conductivity through the tunnel junctions. Dominating cooling mechanism depends on the temperature range and particular CBT characteristics.\textsuperscript{13} Most often, however, at the temperatures under discussion electron thermalization occurs via energy transfer through electron-acoustic phonon interaction. A heat flow between electrons and phonons is given by the expression\textsuperscript{14,15}

\[
P_{el-ph} = \sum \Omega (T_{el}^n - T_{ph}^n),
\]

where $T_{el(ph)}$ is the temperature of electrons (phonons), $\Omega$ is the volume of the islands, $\sum$ is a material-dependent constant characterizing the electron-phonon coupling in aluminum ($n = 5, \sum \sim 0.2–0.3 \times 10^9$ W m\(^{-3}\) K\(^{-5}\)\textsuperscript{12,16} and highly doped degenerated n-type silicon ($n = 6, \sum \sim 2–7 \times 10^8$ W m\(^{-3}\) K\(^{-6}\)\textsuperscript{10,17,18}). Weak electron-phonon coupling due to the strong temperature dependence in Eq. (6) is very well known to be the bottleneck in the heat transfer below 1 K that effectively precludes electrons from reaching full thermal equilibrium with phonons, especially in the millikelvin range. Any voltages either applied or parasitic, e.g., dc bias, ac excitation, electromagnetic noise, etc., lead to heat dissipation, and hence, higher effective electron temperatures unless the electron-phonon coupling is strong enough to ensure full electron thermalization. As was mentioned above, both width and depth of the conductance dip are related to the electronic temperature measured by a CBT. However, the width or rather the entire shape of the conductance dip is affected by different temperature dependent processes in electron tunneling. These are difficult or even impossible to control experimentally or take into account when interpreting the conductance dip. Apart from the self-heating caused by the external and parasitic signals and noise, temperature dependence of the tunnel barrier height and its asymmetry with respect to the applied voltage polarity add more to the ambiguity in interpretation of CBT tunneling conductance. Assumptions are required about exact mechanisms of physical processes involved which are not always fully justified and adequate. Very often arbitrary fitting parameters are introduced when simulating the conductance dip and deriving temperature values from its width. In our case of a hybrid CBT structure containing islands of different materials (silicon and aluminum) guessing about exact mechanisms of the electron thermalization is even less straightforward. Therefore, further we derive CBT temperature from the relative depth of the conductance dip $\Delta G/G_T$ related to zero-bias $G$ value. Figure 3(a) shows $\Delta G/G_T$ for the CBT as a function of the bath temperature. In addition, linear fit to the experimental data (Eq. (3)) as well as with the correction terms up to the 3rd order (according to Eq. (5)) are presented by the dashed-dot and dashed curves, respectively. As it follows from the figure, agreement between the 3rd order theory and experiment is rather good down to ~50 mK. Below this temperature, the experimental points are seen to deviate from the theoretical curves tending to saturation around the terminal 12 mK. This clearly indicates that even at zero bias voltage self-heating caused presumably by electromagnetic noise was high enough to keep the electron system out of equilibrium with phonons. Weak electron-phonon coupling rapidly

![FIG. 2. CBT differential conductance vs. dc bias measured at different bath temperatures (a). The conductance exhibits a dip at bias voltages close to zero due to the temperature dependent Coulomb blockade in electron tunneling. (b) A theoretical curve (red) calculated using model Eq. (1) and fitted to the experimental dip measured at 206 mK.](image-url)
decreasing with lowering temperature according to Eq. (6) is assumed to hinder effective electron thermalization at sub-50 mK temperatures. Besides, at the lowest temperatures the CBT enters the range where charging energy $E_C > k_B T$ approaching the regime of full Coulomb blockade. In this regime, tunneling conductance becomes less sensitive to temperature being determined eventually by the charge fluctuation on the islands of the CBT array.\(^3\) Under the electromagnetic noise conditions in our experiments and with the current CBT circuitry design, the virtual decoupling of electrons from phonons at low temperatures limited the range where the CBT can provide reliable and precise temperature measurements. Figure 3(b) shows the thermometer calibration curve in terms of temperature measured by the CBT, $T_{\text{CBT}}$, as a function of bath temperature. $T_{\text{CBT}}$ was derived from the relative depth of the experimental conductance dip $\Delta G/G_T$ (Fig. 3(a)) using Eq. (5) and charging energy $E_C/k_B = 50$ mK. Linear dependence $T_{\text{CBT}}(T)$ indicates a good agreement between the temperatures in the wide range from $\sim 500$ mK down to $\sim 65$ mK spanning almost one order of magnitude.

In summary, in the present work we have demonstrated that primary Coulomb blockade thermometry can be implemented on a semiconductor material platform. CBT fabricated using highly doped silicon-on-insulator was shown to provide high precision measurements at millikelvin temperatures with a wide dynamic range limited at the low end by the partial electron thermalization due to weak electron-phonon coupling. Recently, an advanced state-of-the-art all-metal CBT device operating at temperatures down to 10 mK has been demonstrated.\(^1\) In our case of rather proof-of-concept prototype, no special attention was paid to the device circuitry design with respect to the electromagnetic noise immunity and enhanced electron thermalization. Good performance demonstrated for such a trivial and straightforward CBT topology as that attempted in this work bears particular promise for further advance through the implementation of system design with enhanced noise immunity and electron thermalization. The great advantage of the silicon-based approach is that it is fully compatible with very well developed contemporary silicon technology dominating on the market. With all the highly developed microfabrication tools available in a modern cleanroom, Coulomb blockade thermometry can be easily implemented in a variety of silicon-based devices, architectures and solutions compatible with industry oriented paradigms, such as very large scale integration and mass-production.


