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Full-Duplex Wireless Transceiver Self-Interference Cancellation Through FD-SOI Buried-Gate Signaling

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Abstract—Full-Duplex (FD) transceiver architectures have recently gained increased attention due to their potential for doubling the theoretical spectral efficiency. One of the main challenges in FD transceivers is the self-interference (SI) from the local transmitter (TX). In this paper we present a novel analog SI cancellation technique through buried-gate signaling in the fully-depleted silicon-on-insulator (FD-SOI) process. The proposed technique attenuates the TX leakage in the receiver (RX) chain before gain is applied. This relaxes the dynamic range requirement of the later RX stages by the amount of attenuation offered by the buried-gate signaling. Further, in comparison to other published analog techniques, the proposed technique offers no penalty on RX noise figure. Measured results in a 28nm FD-SOI technology demonstrate 40-50dB of SI cancellation for TX leakage as high as -10dBm, and above 20dB for TX leakage of -5dBm, with no increase in the RX noise figure.

I. INTRODUCTION

The ever-growing demand for increased data rates in today's overcrowded wireless spectrum has led to the development of spectral efficient system concepts. One such concept to gain considerable attention is the full-duplex (FD) transceiver architecture. FD transceivers have the ability to transmit and receive simultaneously, thereby potentially doubling the system data-rate [1]. One of the main challenges faced in FD transceivers is local transmitter (TX) signal leakage to the receiver (RX). This is commonly referred as self-interference (SI). SI can originate from the direct path between transmit and receive antennas, substrate coupling, and the reflection paths created by transmissions scattered from nearby objects [2].

Figure 1 depicts the block diagram of a typical single antenna FD transceiver. The severity of SI in such a FD transceiver can be best comprehended with a quantitative example of long-term-evolution-advanced (LTE-A) technology. The specified transmitted power for LTE-A user equipments is 23dBm [3]. To overcome the TX leakage from such transmitted powers, either circulators or duplexers are implemented in FD systems. Commercial duplexers can provide an attenuation of around 50dB [4]. However, the lack of wideband tunability in these minimize their use in programmable software-defined-radios. On the other hand, circulators provide wide-

Fig. 1. TX signal leakage or self-interference (SI) in full-duplex transceivers.

band operation but have a limited attenuation of 15-20dB. If we assume a 20dB circulator implementation for a more challenging SI leakage scenario, the circulator will reduce TX leakage down to the level of +3dBm at the receiver input. Assuming the sensitivity level of -97dBm for LTE-A band 1 with 10MHz baseband bandwidth, the required dynamic range of RX can be calculated as 100dB. This creates unnecessarily high requirements for receiver linearity. Consequently, canceling transceiver SI becomes quite critical for reasonable RX linearity specifications.

Ideally, in order to reduce the dynamic range requirements of later RX stages, SI should be canceled as early as possible in RX chain. This has resulted in various analog SI cancellation techniques where cancellation is performed at the input of RX chain [2], [5]–[9]. However, SI cancellation at RX input comes at the penalty of increased noise figure (NF) due to additional SI cancellation circuitry. In this paper we present a novel analog technique for SI cancellation which does not degrade RX noise figure. The technique utilizes the buried-gate (BG) terminal of fully-depleted silicon-on-insulator (FD-SOI) technology for SI cancellation, rather than just dc biasing of transistors. A weighted and 180° phase shifted TX signal is applied to the buried-gate terminals of designed RX low noise amplifier (LNA) to cancel the TX signal at LNA output. Measured results on 28nm FD-SOI technology demonstrate around 40-50dB of SI cancellation for TX leakage as high as -10dBm and above 20dB for TX leakage of -5dBm with no

increase in the RX NF.

Although our proposed implementation performs the TX cancellation at LNA output, nothing prevents using the proposed technique also in baseband amplifiers. This will provide additional SI cancellation on top of the 40dB in the LNA and will further relax the linearity requirement of later RX stages. As this design was implemented as proof of concept, we did not implement the buried-gate cancellation path in baseband amplifiers.

The paper is organized as follows: Section II details the prior-art techniques for SI cancellation in FD systems. Section III explains the basic operation of buried-gate or body-biasing in FD-SOI technology, together with gain simulation results for a single FD-SOI transistor. Section IV describes the RX front-end design and measured results while Section V concludes the paper.

II. SELF INTERFERENCE CANCELLATION TECHNIQUES

SI in FD systems generally falls in two categories [1]: First, the direct leakage from TX to RX, which mainly originates through duplexer/circulator leakage path and substrate coupling. Second, the leakage caused by delayed reflected TX components from the environment. Both of these SI categories can be canceled through analog and/or digital techniques. However, due to the varying nature of environmental reflected signals, such SI requires complex algorithms and detailed multipath reflections modeling for cancellation, and is therefore, more easier to implement in digital domain [2]. However, solely digital SI cancellation techniques require huge dynamic range of RX and analog-to-digital converter (ADC). To mitigate this problem, various analog-domain solutions which cancel the SI earlier in RX chain have been implemented in conjunction with digital domain cancellation [2], [5]–[9].

One of the main problems with the current analog cancellation techniques is the RX noise figure (NF) increase due to the analog SI cancellation circuitry. In this paper, we have presented a novel technique, for direct SI cancellation, through buried-gate signaling in FD-SOI process which has no penalty on RX NF and can be used in conjunction with the digital techniques. In the next section we will cover the details of buried-gate signaling specific to FD-SOI process and how it is used in our implementation for SI cancellation.

III. BURIED-GATE IN FD-SOI PROCESS

The FD-SOI technology offers improved performance together with lower production costs compared to typical bulk CMOS technology [10]–[14]. Figure 2 shows simplified transistor structure of the FD-SOI technology. The transistor differs from the conventional bulk CMOS transistor by the addition of ultra-thin buried-oxide. The presence of this layer allows the possibility to isolate the substrate/body below the transistor channel. This brings clear advantages of reduced leakage currents, higher operating speeds, and the possibility to use body terminal as a buried-gate. The buried-gate can be utilized as a second gate that controls the current flow in the transistor channel by applying of different dc-bias voltages. As

Fig. 2. Structure of transistor in FD-SOI technology

Fig. 3. Comparison of signal normalized gain and phase through the gate and buried-gate for a single FD-SOI transistor.

a result, transistor performance parameters such as threshold voltage, etc. can be tuned for either higher speed or low power consumption [15].

In this paper, we utilize the above buried-gate control of FD-SOI transistor on channel current for RF signal processing rather than just dc-biasing. The RF signal applied at the buried-gate terminal is a weighted and 180° phase shifted replica of the TX leakage signal, which when combined with the main-gate signal cancels the SI at LNA output.

Figure 3 shows simulation results of gain and phase response comparison when two signals at the same frequency are applied at a single transistor gate and buried-gate. It can be seen that the signal path from the buried-gate to the output has a clear signal loss. This makes the buried-gate terminal unsuitable for typical amplifier design. Nevertheless, the results demonstrate that if the buried-gate signal is sufficiently amplified, it can be utilized to cancel the TX signal appearing at the input of RF front-end. This is easy to achieve in FD systems, as the generated TX signal is already much stronger in amplitude than the received TX leakage at the front-end input. Therefore no further amplification is required to utilize the signal for buried-gate SI cancellation. Rather in some cases, attenuation may be required to suppress the TX signal.

IV. CIRCUIT DESIGN AND MEASUREMENTS

To evaluate the proposed SI cancellation technique, an RF front-end was fabricated in 28nm FD-SOI technology consisting of an LNA, N-path downconversion filtering and BB amplifiers. The front-end occupied an active area of 0.2mm² and was tuned for a gain of 40dB and BB bandwidth of 10MHz to test an LTE-A use case. Figure 4 shows the implemented LNA for evaluating the proposed technique. The LNA consists of push-pull common-gate (CG) common-source (CS) stages

Fig. 4. CG-CS LNA with buried-gate signaling.

with capacitive feedback for impedance matching. The CS stage is added to increase the output impedance of the LNA which is required for proper functioning of the N-path filtering, as it affects the relative blocker attenuation [16]. The output common-mode voltage is stabilized through a opamp based feedback which is omitted for simplicity. A weighted and 180° phase shifted TX signal is ac-coupled to the buried-gates of the transistors, while the dc-voltages for the buried-gates are set to meet the optimum threshold voltages of the transistors.

Figure 5 details the measurement setup. An off-chip output buffer was added to avoid BB stage loading from spectrum analyzer. The TX leakage signal was generated by an Anritsu dual output phase coherent signal-generator and provided at the LNA input. Further, a weighted and 180° phase shifted replica of the leakage was provided at the buried-gate input for SI cancellation. Here, an additional Minicircuits amplifier ZX60-14012L-S+ with 5dB NF was added in the buried-gate signal path to emulate the noise present in real on-chip SI cancellation circuitry.

Figure 6 shows the measurement results for comparison between normalized front-end gain when the TX cancellation is off and when its on. Measurement was performed for a CW signal at different frequency offsets from the local oscillator (LO). The relative gain and phase between gate and buried-gate were adjusted to obtain maximum attenuation. It can be observed that around 40dB of SI cancellation is achieved. In Figure 7, a worst case scenario for LTE-A is tested when the TX duplex distance is at minimum of 30MHz. A desired in-band CW signal of -65dBm is provided at a 1MHz offset from the LO and TX signal of -40dBm is provided at a 30MHz offset from the LO. The following key points can be observed from Figure 7: First, the TX signal is attenuated by 40dB when TX cancellation is on. Second the desired in-band signal gain remains the same, and third, no increase in the in-band noise

Fig. 5. Measurement setup for the proposed SI cancellation technique.

floor is observed. More precise NF measurements using the noise diode Y-factor method were also carried out to confirm this: no penalty in RX NF.

In Figure 8, measured maximum SI attenuation for different TX leakage powers is plotted. Around 40-50dB of SI cancellation is observed for TX leakage powers as high as -10dBm and above 20dB for TX leakage of -5dBm. The decrease in SI attenuation at high TX leakage can be attributed to limited input linear range in the LNA.

In Figure 9 and 10, measured normalized front-end gain is plotted for different phase and relative gain (G_{rel}) settings. Here, G_{rel} is defined as the ratio between buried-gate and gate input powers: $G_{rel} = P_{buriedgate}/P_{gate}$. The results suggest a need for accurate phase and amplitude tuning requirement for SI cancellation. To achieve such accurate tuning, algorithms can be implemented in the digital domain which measure the TX leakage at the LNA output and adjust the gain and phase of the buried-gate cancellation path for maximum attenuation. Implementation examples presented in [5]–[7] demonstrate how to generate required phase and amplitude tuning.

In Figure 11 normalized RX gain is plotted for an LTE-A 10MHz modulated signal. The signal is provided at LTE-A minimum duplex distance of 30 MHz. Around 20dB of SI attenuation is achieved for modulated signal. Due to inability of Anritsu signal generator to generate phase coherent LTE modulated signals, above measurement was performed using off-the-shelf coarsely tuned phase-shifters and attenuators. This explains why the SI cancellation is limited to 20dB for modulated signal case. We estimate better SI cancellation for more precise phase and gain tuning in measurements.

V. CONCLUSION

TX signal leakage or self-interference (SI) is one of the key problem in full-duplex transceivers. In this paper, we proposed a novel analog SI cancellation technique using the buried-gate terminal of FD-SOI technology. The measured results for the fabricated front-end in 28nm FD-SOI technology demonstrated around 40-50dB SI cancellation for TX leakage powers as high as -10dBm and above 20dB for TX leakage of -5dBm. Compared to other analog SI cancellation techniques, the results demonstrate no NF degradation from the SI cancellation

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work	[5]	[7]	[8]
TX cancellation (dB)	20-50	30-68	20-23	55
NF increase (dB)	no increase	<0.8	1.2	1.55
RF frequency (GHz)	0.7-2.0	0.3-1.7	1.92-1.98	1.7-2.2
TX cancellation config Active/Passive	Passive	Active	Passive	Active
Front-end power consumption ⁽¹⁾ (mW)	11	-	10	-
Process/V _{DC}	28nm FDSOI/1V	65nm CMOS	40nm CMOS/1V	40nm CMOS/1.2V

1) Excluding LO buffering

Fig. 6. Measured normalized TX leakage signal gain vs BB frequency. Around 40dB of SI cancellation is observed for a CW signal test case.

Fig. 7. Comparison between measured BB spectrum when SI cancellation is turned on and turned off. The BB bandwidth is set to 10MHz for an LTE-A use case, with TX leakage at the shortest duplex distance of 30MHz. Around 40dB SI cancellation is observed.

Fig. 8. Measured SI cancellation for a CW signal at different TX leakage powers.

circuitry. The proposed technique has been applied to only LNA circuitry as a proof of concept. However, the idea can be easily extended also to baseband amplifiers for additional

Fig. 9. Measured normalized gain vs phase between gate and buried-gate signals.

Fig. 10. Measured normalized gain vs relative gain between gate and buried-gate signals.

Fig. 11. Measured normalized gain for 10MHz LTE modulated signal. Around 20dB SI cancellation is achieved when the buried-gate signaling is on and when its off.

SI cancellation.

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