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Fault tolerant design and analysis of carbon nanotube circuits affixed on DNA origami tiles

Eugen Czeizler and Pekka Orponen,

Abstract—Due to its programmable nature, DNA nanotechnology is currently one of the most advanced and most reliable self-assembly based methodology for constructing molecular-scale structures and devices. This makes DNA nanotechnology a highly promising candidate for generating radically new manufacturing technologies. Our specific interest is in the use of DNA as a template and scaffold for the self-assembly of Carbon-Nanotube Field Effect Transistor (CNFET) circuits. In this research we introduced a novel high-level design framework for self-assembling CNFET circuits. According to this methodology, the elements of the circuits, i.e., CNFETs and the connecting carbon nanotube wires, are affixed on different rectangular DNA scaffolds, called tiles, and self-assemble into the desired circuit. The introduced methodology presents several advantages, both at the design level, and for analyzing the reliability of these systems. We make use of these advantages and introduce a new fault-tolerant architecture for CNFET circuits. Then, we analyze its reliability both by computer simulations and by analytical methods.

Index Terms—Circuit analysis, circuit reliability, circuit topology, CMOSFET circuits, algorithms, biological materials, circuit simulation, combinatorial mathematics, DNA

I. INTRODUCTION

RECENT years have witnessed a burst of experimental activity concerning algorithmic self-assembly of DNA nanostructures, motivated at least in part by the potential of this approach as a radically new manufacturing technology [1], [2], [3], [4]. In particular, one of the most promising design approaches, is based on the use of synthetic DNA as a template/scaffold for the desired assembled structures [5], [6], [7], [8].

One of the currently most reliable programmable self-assembling nanostructure architectures is DNA origami [9]. This method involves the folding of a long single-stranded DNA sequence with the help of several shorter “staple” strands. In this way, highly complex patterns can, and have been, experimentally achieved, with an unprecedented high level of accuracy and reliability. Moreover, several authors have announced the formation of DNA origami tiles capable of further assembly into larger, fully addressable, 1D and 2D template lattices [10], [11], [12]. Such scaffolds make possible the construction of highly complex structures on top of them [6], [10], [13], [14], prospectively including nanocircuits. Our specific interest is in the self-assembly of Carbon-Nanotube Field Effect Transistor (CNFET) circuits.

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Single-wall carbon nanotubes (CNT) can be either metallic (m) or semiconducting (s). A cross-junction between an m- and an s-type CNT generates a structure with experimentally proven field effect transistor (FET) behavior [1], [15], [16], [17]. This way, both P-type and N-type FETs are realizable: a P-type FET is ON when its input signal is “0”, while an N-type FET is ON when its input signal is “1”.

The reporting in 2002 of a programable attachment of DNA strands onto individual CNT [18], followed one year later by the first demonstration of a back-gated CNFET with source and drain leads using metallized DNA strands [19], has generated considerable interest of the research community over the possible development of DNA-guided CNFET nanoelectric circuits. Following results addressed both the development of appropriate design architectures for such circuitry [16], [20], [21], as well as experimental achievements of various nanoelectric prerequisites, including nanowire fabrication and attachment to DNA scaffolds [22], [23], metallization, and creation of interconnects [24], [25], [26], etc. . Initially, such circuits were conceptualized on top of addressable DNA lattices [6], [8], [16], with individual CNT and interconnects placed on precise locations of such DNA-breadboards. While such large lattices (2–5 μm) are experimentally achievable [2], [11], [27], the uniformity of their structure as well as the fact that the entire circuit must assemble simultaneously, has the potential of creating significant difficulties in the overall functionalization of these lattices. After the introduction of the DNA origami technique, researchers concentrated over the integration of elemental nanoelectric components on top of these individualized structures [1], [5]. Current developments in the field are particularly achieving a high level of accuracy [10], [13]. Two recent surveying presentations on the topic of DNA-assisted nanoelectric circuitry are [6], [8].

In the current research we propose a generic framework for the design of CNFET circuits on top of modularized independent scaffolds, such as individualized DNA origami tiles. According to this framework, the elements of the circuits, i.e., CNFETs and the connecting carbon nanotube wires, are affixed on different rectangular DNA scaffolds, called tiles, and self-assemble into the desired circuit. In particular, we introduce a “universal” set of such tiles such that with a proper selection of linkers for these tiles, also known as “glues”, any desired CNFET circuit can be self-assembled from this basis.

As we show in the following sections, the present design framework possesses several considerable advantages: it allows for a structured and clear design; it uncouples the self-assembly aspects of the manufacturing process from the transistor circuit design; and, it also supports efficient high-level

analysis of complex circuits, both by computer simulations and by analytical approximation methods. For instance, all assembly errors can be treated at this level as tiling errors, thus leading to a transparent design discipline for fault-tolerant architectures.

The paper is structured as follows. In the next section we providing basic electrical engineering notions concerning the design of CMOS circuits, introduce our design framework for CNFET circuits, and discuss its advantages. In Section 3 we consider the issue of fault-tolerance in electrical engineering and introduce our design strategy for fault-tolerant CNFET circuits. Section 4 is devoted to analyzing the reliability of the CNFET fault-tolerant circuits, in comparison with the non fault-tolerant designs. We apply at this level both a computational approach as well as an analytic approximation method for assessing the reliability of our designs. Section 5 is devoted to discussions and conclusions.

II. CNFET CIRCUITS AFFIXED ON DNA ORIGAMI TILES

In this section we introduce our design framework for CNFET circuits, and present its advantages. We start by giving a few basic electrical engineering notions, particularly concerning the design of CMOS circuits.

A. Basic principles of CMOS circuit design

We restrict ourselves to the case of CMOS (complementary-symmetry metal-oxide semiconductor) digital circuit design technology. In this framework, a circuit is composed of P-type and N-type transistors, i.e., metal oxide semiconductor field effect transistors (MOSFETs), connected by wires and implementing logic functions. One of the main advantages of CMOS technology is that it assumes a discrete separation of the voltage levels. Thus, a logical “1” corresponds to electrical level Vdd, i.e., the power source, while a logical “0” corresponds to GND, i.e., ground or 0V.

In this research, we are going to restrict to the simplified case where transistors are thought of just as ON/OFF voltage-controlled switches. Both P-type and N-type transistors have a gate, drain, and source terminal, see e.g. Fig. 1. The gate terminal can be seen as the transistor’s input since, depending on its voltage and the transistor type, it switches the flow of electrons on and off between the source and the drain. Thus, a P-type transistor is open (or switched OFF) when the gate voltage is “1”, i.e., the gate is connected to Vdd, and it is closed (or switched ON) when its gate voltage is “0”, i.e., the gate is connected to GND. The N-type transistor has an opposite behavior: it is switched ON when its input is “1” and OFF when its input is “0”. The typical CMOS design uses complementary and symmetrical pairs of P-type and N-type MOSFETs such that at each time, each of the outputs of a (sub)circuit is either “1” or “0”, i.e., either connected to Vdd or to GND. If at any time point, either due to bad wiring or due to some errors, a connection between the Vdd and GND electrical levels is established, possibly routed through several ON P-type and N-type transistors, then we have a short circuit. This leads to power dissipation and may induce the physical damage of the circuit.

Fig. 1. The representation of a P-type (left) and an N-type (right) CMOS transistor. P-type transistors are differentiated from N-type ones by the presence of a small circle at the gate terminal.

The simplest CMOS circuit is the Inverter gate, Fig. 2 a). If the input of this circuit is “1” then the P-type and N-type transistors are OFF and ON, respectively, thus connecting the output to GND, i.e., the logic “0”. Dually, the output is connected to Vdd, i.e., logic “1”, if and only if the circuit’s input is “0”. Thus, the Inverter is the electronic implementation of the NOT logic gate. Fig. 2 b) presents the slightly more complex implementation of the NAND logic gate, while in Fig. 2 c) one can see one of the possible CMOS designs of a Full Adder, i.e., adding three one-bit numbers and outputting the result in the form of two one-bit outputs.

Fig. 2. The blueprint of CMOS circuit design for a) Inverter, b) NAND gate, and c) Full Adder.

B. A novel design framework for CNFET circuits affixed on DNA origami tiles

In the following we introduce a new high-level design framework for self-assembling CNFET circuits. According to this methodology, the elements of the circuits, i.e., CNFETs and the connecting carbon nanotube wires (CNW), are affixed on different rectangular DNA origami tiles which further self-assemble into the desired circuit.

The central idea is to split a circuit into basic unit-like components such as P-type transistor, N-type transistor, unit straight wires, unit 3- or 4-way junction wire, etc. Each of these basic electronic components are implemented using CNT, and are placed each on top of different rectangular DNA origami structures. Depending on the exact design of a particular circuit, each origami structure is augmented with a set of hanging single stranded DNA (ssDNA) molecules which are used as sticky ends and derive the subsequent assembly of the desired circuit. This second-stage assembly is formalized using the Tile Assembly Model (TAM) [28], a well known tile-based formalism used for the algorithmic design of self-assembling shapes and patterns out of DNA-build tiles.

To this end, we introduce a “universal” set of 14 differentially functionalized DNA origami tiles, each having affixed on

Fig. 3. The 14 tile types and the blank tile, out of which any CNFET circuit can be assembled: a) P-type and N-type CNFETs, b) straight CNWs, c) corner CNWs, d-e) 3- and 4-way CNW junctions, f) crossing but non-interacting CNWs, g) blank tile.

its surface a specific CNT-based electrical subunit. This set, visually described in Fig. 3, consists of P-type and N-type transistor tiles, straight-wire tiles, corner-wire tiles, 3- and 4-junction-wire tiles, and a bridged-wire tile with two crossing but non-interacting wires. In addition, it is convenient to add a blank tile, Fig. 3 g), which is used for filling up inner circuit surfaces, and for analyzing fault tolerant architectures. With a proper selection of “glues” on the tiles, any desired CNFET circuit can be self-assembled from the above tile-basis. This can be inferred easily from Fig. 4, where appropriate designs for the Inverter, NAND, and Full Adder CMOS circuits are implemented. In order to derive an appropriate and efficient selection of glues for these tile, we refer to the Patterned self-Assembly Tile set Synthesis (PATS) Problem [29], [30].

Fig. 4. Examples of CNFET circuit designs: Inverter gate, NAND gate, and Full Adder.

The central elements of the TAM formalism are tiles [28], which are non-rotatable unit square structures, uniquely defined by the sets of four glues placed on top of their edges. Each pair of glues is associated a strength value, determining the stability of the link formed between two tiles having these glues on the abutting edges. In most cases, it is assumed that

the strength of two distinct glues is zero, while a pair of matching glues has strength either 1 or 2. The assembly process starts from a predefined “seed” structure. A tile successfully attaches to an existing assembly if the total strength of all links between the new tile and the existing assembly is greater than a threshold.

In most cases, the type of a tile is determined by the sequence of glues placed on its edges. However, in some cases, tiles can be themselves differentiated, e.g., depending on their functionalization. Thus, we can see such tiles as being colored with colors from a finite alphabet. The PATS problem asks that given a 2D pattern P of colored tiles, to find a minimal set of tile types which self-assemble P . In our case, one can view the previously introduced CNT-functionalized tiles as being “colored” according to their different functionalities. Thus, a circuit C in this framework can be seen as a 2D colored tile pattern, with at most 15 different colors. In order to find a proper (and efficient) selection of glues for the CNT-functionalized tiles which would ensure the self-assembly of C , we just need to apply one of the known algorithms for solving a particular instance of the PATS problem¹. For example, it has been shown in [30] that the self-assembly of the Full Adder circuit from Fig. 4 requires approximately 50 different tile types.

C. Design advantages of the CNFET framework

The high-level design framework introduced here has a number of significant advantages, both relevant for the design of nanocircuits, and for the analysis of their reliability. One of such advantages is that the current approach decouples the self-assembly of the circuit basic components, i.e., the CNFET tiles and CNT unit-wire tiles, from the assembly of the actual circuits. Such components can be manufactured in different test-tubes, at different time stages, in different quantities, etc., and the obtained CNT-functionalized tiles can be preserved without a particular glue initialization. Then, when a particular circuit is to be assembled, a glue-initialization is determined algorithmically and embedded on the already available tiles.

Another advantage of the framework is the clarity and structure of the generated CNFET circuit designs. Given a CMOS circuit blueprint, the construction of the associated CNFET design is straightforward. The scalability of the design represents another important advantage, especially regarding the nanoengineering (and manufacturing) process of these structures. The elements of the circuit, i.e., CNFETs and CNWs, are placed on top of DNA origami tiles. While the current state-of-the-art is that the size of the underlying DNA origami (and thus the size of any of the circuit’s unit elements) is a rectangle of approx. 60×100 nanometers, the circuit design does not depend of this current technology. Instead, if new technologies become available, such as placing the CNT on smaller DNA tiles, or even introducing totally new functionalizations of the DNA origami, e.g., with new types of electrically conducting and semiconducting mediums, the design framework does not need to be itself updated.

¹Note that the PATS problem has been described as NP-hard, see [31]

Finally, another significant advantage of our methodology, is that the design framework supports efficient high-level analysis of the purported circuits, both by computer simulations and by analytical approaches. This is because all the assembly errors at this level can be treated as tile-substitution errors, thus leading to a transparent design discipline for fault-tolerant architectures. Let us consider, for example, a three junction tile type, Fig. 4 d). If the functionalization of one particular copy of such a tile would be faulty and the (shorter) vertical CNTs would fail to be positioned on the tile, then this particular tile will act as a straight horizontal wire tile, such as those from Fig. 4 b). Similarly, if the functionalization of this DNA origami responsible for connecting the CNW with a neighboring CNW (from a different tile) would get faulty, then, the tile will act as a corner tile (the direction of the corner would depend on the position of the faulty functionalized element). In the worst situation, if the functionalization of a tile is highly altered, the tile can be considered a blank-type tile. The following sections are devoted to the design and analysis of fault tolerant architectures which are constructible in this framework.

III. FAULT TOLERANT DESIGNS OF CNT CIRCUITS

An intrinsic property of nanostructures, self-assembled ones in particular, is a high density of defects and assembly faults. Thus, a major concern while engineering such systems is the embedding of effective fault tolerant architectures within these designs. Indeed, such architectures have been intensively studied in connection to various dynamical nanosystems, such as for DNA-tile assemblies [32], [33], for fault-tolerant designs for nanowire-based programmable logic arrays [34], or for reliable nanoelectronics [35]. During this section, we introduce a fault-tolerant technique for CNFET circuits, and analyze its effect over the reliability of the generated circuits. A short analysis of various different approaches achieving fault tolerance in electrical engineering is presented in Supplementary Note 1.

In order to implement fault-tolerant CNFET circuits we are adapting the classical approach based on the Quadded Transistor Structure (QT-structure) [36], [35]. In there, each CMOS transistor (either of P- or N-type), is replaced by a 2×2 transistor structure, where pairs of transistors are placed both in series and in parallel. We select this particular technique for two reason. First, because such a low-level implementation of fault-tolerance, i.e., at the transistor level, is documented to be more efficient in the case of circuits with high defect densities [35], as expected in the case of DNA-scaffolded structures [1], [5], [14]. The second reason is that in the case of CNFET circuits, both the transistor and the wire components are similarly vulnerable to errors. Indeed, since the unit elements of our circuits are either CNFETs or CNWs functionalized DNA tiles, any of these elements has a similar defect probability. Because of its design, the QT-structure can be updated easily for achieving fault tolerance both at transistor and at wire level. As a general strategy, we implement the wire fault tolerance by replacing each wire by a pairing of two parallel and bridged wires.

As previously mentioned, one of the main advantages of our framework is that all the errors affecting the circuit can be ultimately treated as tile-substitution errors. From practical considerations, we assume in the following a *blank-error model*, where each erroneous tile from the assembly is replaced by a blank tile-type. Some other possible ways of implementing the error-triggered tile substitutions are discussed in Supplementary Note 2.

Our fault tolerant designs for the CNFET circuits are implemented using a customary modification of the QT-structure technique, complemented by a wire defect-tolerant architecture.

Fig. 5. The implementation of the Quadded Transistor structure for the tile-based CNFET circuits. The QT-structure above is replacing a P-type transistor from the original circuit.

Thus, each CNFET-tile is replaced by a 4×4 CNFET QT-structure, incorporating 4 similar CNFET tiles, see Fig. 5. Similarly, each linear sequence of CNW-tiles implementing a wire is replaced by a width-2 ribbon structure, implementing a paired and bridged wire. In Fig. 6 we present the fault-tolerant designs of the Inverter and the NAND gate CMOS circuits; the fault-tolerant design of the Full Adder circuit is presented in Supplementary Fig. 1.

Fig. 6. Two fault-tolerant CNFET circuits implemented using the QT-structure: a) Inverter, b) NAND gate.

By using the QT-structure, as well as the width-2 ribbon structure, we make sure that any single tile error within the assembly, i.e., a blank tile substitution of the tile in case, is well tolerated at the circuit level. However, one can easily observe that such a circuit architecture has a stronger fault-

tolerant effect. In particular, any sum of single tile errors within different QT-structures, as well as any sum of tile errors within a width-2 ribbon structure where the errors are placed at least two tiles apart, is still tolerated by the circuit. For example, for the NAND circuit in Fig. 6 b), the fault-tolerant architecture can tolerate up to 21 uniform-distributed tile-errors, without affecting the circuit's overall output function.

If required, circuits can be designed to achieve even stronger tolerance to errors, by using the N^2 transistor-structure [37], a generalization of the QT-structure, see Supplementary Note 1. In Supplementary Fig. 2 we present the N^2 -design of an Inverter and NAND gate, for the case $N = 3$, while in Supplementary Note 4 we analyze the reliability of these circuits.

TNano, a Graphical User Interface for the design and analysis of CNFET circuits

In order to ease the design process of CNFET circuits, we have employed the use of a customary created Graphical User Interface (GUI), T-Nano [38]. The primary purpose of this interface is to provide an easy, graphical medium, for the design of CNFET tile-based circuits. However, some basic tools, such as simulation of the circuit and basic fault-tolerant analysis, are also incorporated into the GUI. Available features of the GUI include: graphical tile selection and placement onto the 2D grid; cut, copy, and paste functions for partial patterns in the circuit; zoom in/out from the current working sheet; multi-window working, etc. Also, the GUI provides a pdf export option for the generated circuits, see e.g. Supplementary Fig. 1 and 2 generated by the software. The GUI proved to be particularly useful for the design of medium and large scale CNFET circuits, such as the Full Adder, the fault-tolerant NAND, and the fault-tolerant Full Adder circuits.

IV. THE RELIABILITY OF CNFET FAULT-TOLERANT CIRCUITS

Deriving an exact analytic formula for the reliability of a given circuit is an unattainable task, even when considering the simplified blank-error model assumptions and medium-sized circuits. This is because in order to determine such a formula, one has to compute the exact error probability of a circuit assuming all possible scenarios, namely when it contains one, two, etc., or all of its tiles, switched to blank tiles.

Let us consider for example the quadded CNFET structure itself from Fig. 5. If only one tile is switched to a blank tile, then the circuit is still working accurately, independent of which tile is switched; we assume that input, output, and voltage tiles are not defective, as they stand for reliable interconnects. If two tiles are switched to blank tiles, out of the total 120 possible pairs, 68 of them will determine the malfunction of the circuit. For three defective tiles, even for this simple case, it is already difficult to compute the percentage of faulty circuits, compared with non-faulty ones. For more complicated circuits, it is practically impossible to compute an exact analytic formula for those triples of tiles who's error would generate a faulty circuit. Thus, in order to determine the reliability of our circuits we employ two

approximation strategies. First, is to consider a computational CNFET simulation tool for approximating the circuit's error probability. Second we derive an analytic approximation formula for circuit reliability.

Our CNFET circuit simulator algorithm is adapted from a classical switch level simulation algorithm for MOS circuits due to Bryant [39] and integrated in the TNano GUI. Some more details regarding its implementation and usage are presented in Supplementary Note 3.

Providing exact analytic formulas for the error probability of CNFET circuits is an unfeasible task, due to the intricate combinatorial aspects needed to account for all possible tile-error combinations. However, generating analytic approximations for such error probabilities is achievable. Indeed, our fault-tolerant designs based on the QT-structure (and generalized for the N^2 -transistor structure) have the property that any one tile error (resp. any combination of $N-1$ tile errors) is tolerated by the circuit. Moreover, only local combinations of two (resp. N) tile errors either along a wire structure or inside a QT-structure, are actually generating circuit level errors. Thus, a possible way of approximating the overall circuit error probability is to count (or approximate) the number of minimal-sized tile-error combinations generating a circuit error.

The analytic formula for the approximate error probability of a fault-tolerant CNFET circuit implemented using the QT-structure is inferred bellow, where: ϵ is the individual tile error probability, W is the number of wire-tiles (approximated in practice as 80% of the tiles not included into a QT structure), and T is the number of QT-structures within the circuit.

$$P_{CE} \approx 1 - (1 - \epsilon(1 - (1 - \epsilon)^3))^{W/2} \cdot ((1 - \epsilon)^{20} + 20\epsilon(1 - \epsilon)^{19} + 190\epsilon^2(1 - \epsilon)^{18} \cdot 0.72)^T \quad (1)$$

The derivation of the above formula is performed in Supplementary Note 4, together with a generalized result for fault-tolerant CNFET circuits implemented using the N^2 -transistor structure.

A. Results

We employ our CNFET circuit simulator algorithm to computationally determine the comparative reliability of regular and fault-tolerant CNFET circuits using the QT-structure and the 3^2 -transistor structure, for the Inverter, NAND gate, and Full Adder circuits. The results of the simulations are described in Fig. 7 a), b), and c), respectively. The same figures contain also the comparison with the prediction generated by the analytic approximation formula (1) for the reliability of fault-tolerant CNFET circuits using the QT-structure. A similar comparison is performed in Supplementary Note 4 for the analysis of regular vs. fault-tolerant CNFET circuits using the N^2 -transistor structure, for the case when $N = 2$ and $N = 3$.

In order to analyze a circuit's overall reliability, we have sampled the individual tile error probability ϵ for values within the interval $[0.001 \ 0.1]$, using a 0.004 step increment. For each circuit C and individual tile error probability ϵ , we computed the circuit's reliability based on 1000 independent simulations of error "bombarded" copies of the circuit. We computed the

Fig. 7. Circuit overall error probability as a function of tile error probability for a) Inverter, b) NAND gate, and c) Full Adder. In each case, the comparison is done between the normal and fault tolerant (based on QT-structure and 3^2 -transistor structure) designs. The analytic approximations are based on formula (1), approximating the error tolerance of circuits whose designs are based on the QT-structure.

average and the standard deviation of these data point in order to report the circuit's overall error rate and its confidence interval, respectively.

V. CONCLUSION

We have introduced a high level design framework for CMOS-based nanoelectric Carbon Nanotube Field Effect Transistor (CNFET) circuits. The design is a tile-based modular implementation, where individualized DNA scaffolds, called tiles, are functionalized either with a P- or an N-type transistor or with a straight/curbed/junction wire. We

have provided a universal set of 14 such functionalized tiles, such that any CMOS-based electric circuit can be assembled from this set, by adding to the tiles some appropriate set of connecting sticky ends, called glues [29].

The currently introduced design framework has a considerable number of advantages. First, it decouples the circuit design task from the design of the underlying DNA lattice. Indeed, all of the 14 different functionalized tiles can be assembled at any time moment before a particular CNFET circuit is envisioned, without placing any glues on these tiles. Then, when some particular circuit is chosen, the CNFET blueprint pattern is generated, and based on it we can compute the appropriate sets of glues to be attached to the functionalized tiles. Thus we generate a tile set designed particularly for assembling the considered circuit, and only that.

The scalability of the design is another of the framework advantages. Even though DNA Origami tiles tend to be rather large ($100 \times 100nm$), minimizing the entire circuit is a matter of nanotechnology advances in creating smaller such origami scaffolds, and functionalizing them with the corresponding nanotubes. Indeed, recent research has experimentally generated smaller DNA origami structures, including some rectangular patterns of approx. $20 \times 20nm$ [40].

Another advantage of our methodology refers to the modularity of the design framework. Since the units of our designs are rectangular tiles, each with its own functional purpose, i.e., either transistor or a connecting wire, the generated circuit blueprints preserve almost entirely the modularity and the elegance of the corresponding CMOS design. Also due to this unit modularity the design framework supports efficient high-level analysis of the CNFET circuits, both by computer simulations and by analytical means. This is ultimately due to the fact that all assembly errors can at this level can be treated as tile-substitution errors, thus leading to a transparent design discipline for fault-tolerant architectures.

We have particularly exploited the above framework advantage and created a dedicated software platform, TNano [38], for CNFET-circuit simulation and analysis of circuit reliability. Moreover, the software platform is complemented by an intuitive graphical user interface for designing and analysing CNFET-circuit blueprints.

In a related direction, we have introduced a special tailored fault-tolerant design technique for CNFET circuits, which we have used to implement a series of fault-tolerant circuits. Using the TNano software platform we have performed detailed analysis and comparisons between the fault-tolerant circuits and their normal (CNFET) counterparts.

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