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Impact of Standard Cleaning on Electrical and Optical Properties of Phosphorus-Doped Black Silicon

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Abstract—Black silicon (b-Si) has been estimated to considerably grow its market share as a front texture of high-efficiency silicon solar cells. In addition to excellent optical properties, high-efficiency cell process requires extreme cleanliness of the bulk material, and thus cleaning of b-Si surfaces is often a critical process step. While standard clean (SC) solution efficiently removes possible contamination from wafer surfaces, we show here that it may cause challenges in b-Si solar cells. First, the silicon etch rate in SC1 solution is shown to depend on the phosphorous concentration and as high rate as ∼1.4 nm/min is observed on planar emitter surfaces. When extending the study to b-Si, which has much larger surface area in contact with the cleaning solution, even higher volumetric Si consumption occurs. This is observed in significant changes in emitter doping profiles, for instance, a 10 and 30-min cleaning increases the sheet resistance from 47 to 57 Ω/□ and 127 Ω/□, respectively. Furthermore, the SC1 solution alters substantially the nanostructure morphology, which impacts the optics by nearly doubling and more than tripling the surface reflectance after a 30 and 60-min immersion, respectively. Thus, uncontrolled cleaning times may impair both the electrical and optical properties of b-Si solar cells.

Index Terms—Black silicon, etching, nanostructure, phosphorus emitter, RCA clean, standard clean.

I. INTRODUCTION

Black silicon (nanostructured silicon, b-Si) is drawing increased interest within the photovoltaic community. The surface texture is able to eliminate reflective losses and is particularly well suited for use with novel diamond wire-sawn multicrystalline wafers, which are unsuited for standard acidic texturing due to the lack of saw damage. Therefore, b-Si has been estimated to substantially grow its industrial market share in the near future [1]. Simultaneously, the PV industry targets ever higher device efficiencies, which imposes more stringent cleanliness requirements for solar cell processing environments.

A key aspect of process contol is to remove surface cleaning prior to high-temperature processing (e.g., emitter formation). This is important especially with specific b-Si fabrication methods, such as metal-assisted chemical etching (MACCE) [2], which introduce contaminants that need to be subsequently removed. Possible contamination sources can be efficiently removed from wafer surfaces by standard cleaning (SC, also called RCA clean) [3]. The same solutions are also typically used to precondition silicon surfaces prior to atomic-layer-deposited thin films to enhance surface passivation [4]–[6]. To reduce the consumption of chemicals and costs, the original two-step process can be compressed into a single step by the addition of a complexing agent (e.g., 1,2-cyclohexanediaminetetraacetic acid, CDIA) into a mixture of ammonium hydroxide (NH₄OH), hydrogen peroxide (H₂O₂), and water (H₂O) which is known as SC1 solution [7], [8]. The effectiveness of SC1 is based on oxide regeneration on Si surface: NH₄OH dissolves the thin native oxide on silicon at a slow rate, while H₂O₂ simultaneously oxidizes the surface at approximately the same rate [3]. After rinsing in deionized water (DIW), the wafers are usually dipped in diluted hydrofluoric acid (HF) to remove a thin oxide which grows during the cleaning. While this mechanism efficiently removes particles and organic contaminants, it may cause challenges for process design of modern silicon solar cells: Cleaning consumes silicon and hence modifies the surface texture and alters the emitter and the optical properties of the surface. While these changes may be considerable already on planar surfaces, the effect of the cleanings is hypothesized to be even more significant in the case of b-Si as a larger surface area is in contact with the chemicals. Although the duration of a single cleaning step is rather short, the total cleaning time accumulating from several cleanings may be considerably long in a complete cell process.

The consumption of Si in SC1 solution with various compositions has been analyzed in several studies [9]–[14]. The reported etch rate have been ∼0.8 nm/min for typically used compositions [10]–[12]. However, the studies have not investigated the effect of SC1 on important solar cell parameters, such as the emitter doping profile.

Some studies have also focused on the effect of HF dips on Si consumption. Ebong et al. observed an increase in phosphorus emitter sheet resistance and decrease in surface doping concentration after an HF dip, which indicated that considerable amount of Si was removed in the solution [15]. Liu et al. studied...
the topic further and discovered that phosphorus concentration affects the etch rate of Si in HF. More specifically, they showed that HF etches phosphorus-doped Si at a surprisingly high etch rate (~0.8 nm/min) when the doping concentration is above $3 \times 10^{20} \text{cm}^{-3}$ [16]. Similar high etch rate in HF has also been reported with heavily arsenic-doped n-type Si [17].

However, it remains ambiguous whether heavy phosphorus doping affects the Si etch rate also in SC1 solution. Furthermore, all past studies have focused only on planar samples, although the surface of a solar cell is always textured, not planar. A surface texture may intensify the effect of the cleanings, and the higher volumetric Si consumption reflect to several important solar cell parameters, such as emitter sheet resistance, morphology of the texture, and the resulting surface reflectance.

In this paper, we investigate the impact of a standard SC1 cleaning solution on silicon consumption using the most typical PV material, i.e., p-type Si with a phosphorus emitter. We give an estimate for the etch rate of phosphorus-doped planar Si in SC1 solution and discuss the physical root cause behind the observed phenomenon. Furthermore, we study the influence of the cleanings on electrical and optical properties of b-Si phosphorus emitters and compare them with p-type b-Si samples without an emitter. Additionally, we expose low-resistivity (0.005–0.01 $\Omega \text{cm}$) phosphorus-doped b-Si wafers to the same treatment to confirm that the etching behavior is not only characteristic to a specific doping method.

II. EXPERIMENTAL

Boron-doped p-type Czochralski (CZ) silicon wafers with (100) orientation and a thickness of 525 $\mu$m were used in the experiments. First, black silicon was fabricated by deep reactive ion etching (DRIE, Oxford Instruments Plasmalab System 100) to some of the wafers (3–5 $\Omega \text{cm}$) using process parameters reported in [18] while the rest of the wafers remained planar (10–15 $\Omega \text{cm}$). After an SC1 cleaning and a dip in 1 wt% HF solution, some of the black silicon and planar wafers were introduced into a diffusion furnace (Centrotherm E1200HT 260-4), where an n$^+$ emitter was formed at 830 °C. POCl$_3$ gas was introduced for 20 min, followed by a 5-min drive-in in oxygen-containing atmosphere. After the phosphosilicate glass was removed by a short 2-min dip in 6 wt% HF solution, initial sheet resistance of the wafers was determined with a four-point probe, of planar samples prior to any cleanings by four-point probe, of planar samples before any cleanings with a four-point probe. The second batch of planar samples replicated the same sheet resistance values within a 2 $\Omega \square$ accuracy, confirming that the SC1 solution remained very stable, as previously demonstrated with low metal contamination level or CDTA addition, which both apply to this study [23], [24].

Sheet resistance was measured with a four-point probe from all emitter samples, both planar and b-Si, to quantitatively characterize the change in the amount of dopants. To estimate the etch rate of heavily phosphorus-doped silicon in SC1 solution, sheet resistances were calculated for ECV profiles truncated near the surface [25]. The amount of silicon removed by the cleaning was determined to be the truncation distance that provided the same calculated sheet resistance value as was experimentally measured. In the sheet resistance calculation, a mobility model from Klaassen was employed [26], [27]. The etch rate was then calculated from the amount of silicon removed and the corresponding cleaning time. To confirm the calculated etch rates, ECV profiles were measured on planar samples cleaned for 10 and 30 min and compared with the original profile. The samples were then dipped in 1 wt% HF until the surface turned hydrophobic (40 s) to reveal a bare Si surface under the thin chemical oxide. The HF dip was kept short enough to prevent additional Si etching after the SC1 cleaning. The evolvement of the nanostructure was characterized by integrating sphere-based surface reflectance measurements (Agilent Cary 5000) and SEM imaging (Zeiss Supra 40).

III. RESULTS AND DISCUSSION

A. Etch Rate

Fig. 1 shows the electrically active phosphorus profiles and the corresponding sheet resistance ($R_{sh}$ values, as measured by four-point probe, of planar samples prior to any cleanings or after SC1 immersion for various times. The sheet resistance values demonstrate a significant reduction in phosphorus concentration with increasing cleaning time, indicating that the surface is indeed etched by the cleaning solutions. Comparison of the experimentally determined sheet resistance and the
corresponding values calculated for the truncated initial profiles imply that 10-, 30- and 60-min cleanings consumed 14 ± 1.5, 36 ± 1.3, and 71 ± 1.3 nm from the sample surface, respectively. The removed regions are highlighted in Fig. 1. Hence, the etch rate of Si was as high as 1.4 ± 0.3 nm/min on average during the first 10 min and slowed down to 1.2 ± 0.2 nm/min for the last 30 min of the 60-min cleaning. The uncertainty results from a 15 s uncertainty in cleaning time, the standard deviation of the sheet resistance measurement (≈1 Ω/□), and a 5% uncertainty in the ECV data. The determined etch rate is significantly higher than ≈0.8 nm/min previously reported for lightly doped surfaces [10]. The ECV profiles measured from the cleaned samples and offset by the calculated etch depths fit well to the original phosphorus profile, which confirms the calculated etch rates. The slight deviation between the profiles of the 0 and 30-min cleaned samples in the region deeper than ≈170 nm can be attributed to the reduced accuracy of the ECV profiling method for low doping concentrations.

The decrease in etch rate as the etching proceeds coincides with a reduced surface phosphorus concentration. Hence, the accelerated Si consumption could be explained by the increased Fermi level which reduces the activation energy required to release an Si atom from the lattice, as in the case of HF [16], [17]. This explanation implies that heavy boron doping would reduce the etch rate as the Fermi level is shifted toward the valence band. However, as the etch rate starts to decrease already after the first 10 min, while the electrically active surface phosphorus concentration remains rather constant for the following 20 min, inactive phosphorus could be another explanation for the accelerated Si consumption. The applied diffusion process is known to result in a considerable amount of inactive phosphorus near the surface, which is not visible in the ECV profile [22]. Hence, also crystal defects (e.g., precipitated phosphorus) could contribute to the accelerated Si consumption. Alternatively, the consumption of silicon could be intensified by lattice mismatch-induced stress in the heavily phosphorus-doped region [16].
increased resistive losses in the emitter and deterioration of Ohmic contacts, resulting in a significantly reduced cell efficiency.

C. Surface Morphology and Reflectance

In addition to electrical properties, surface morphology and the resulting optics are essential parameters for high-efficiency solar cells. Therefore, the impact of the observed high Si consumption in SC1 solution on these properties is further investigated. Fig. 3 presents the evolution of the POCl\textsubscript{3} diffusion-doped b-Si structures in SC1 solution. The SEM images describe separate samples cleaved from a single wafer after the b-Si fabrication and subsequent diffusion. Corresponding images of p-type b-Si without an emitter are shown for reference. In the phosphorus-doped nanostructure, some modifications can already be seen after a 10-min immersion. The change is more significant after a 30- or 60-min cleaning as expected based on the sheet resistance results. Although none of the DRIE-fabricated b-Si spikes is perfectly identical with each other, which is one of the reasons for the excellent optical properties of b-Si [28], the initial nanostructures can be assumed to have been similar on average over a large area in all wafers.

To investigate how the reduction in nanostructure feature size affects the optical properties of b-Si, surface reflectance was next measured from the same samples. Fig. 4(a) presents the surface reflectance spectra of the b-Si emitter wafers. The reflectance increases considerably with increasing SC1 cleaning time: The solar spectrum weighted average reflectance increases from 0.9% to 1.7% and 3.3% during a 30- and 60-min cleaning, respectively. Especially, the deterioration of optical properties is pronounced after a 60-min cleaning. The slight difference in the initial UV range spectra is due to minor differences in the nanostructures caused by the diffusion process. The low reflectance of the low-resistivity samples in the infrared range (wavelengths beyond 1000 nm) is caused by free-carrier absorption [35].

The reflectance spectra in Fig. 4(b) support the observation of heavy phosphorus-doping induced increased Si consumption. Furthermore, the observed phenomenon is not only a feature of POCl\textsubscript{3}-diffused surfaces since a similar behavior is observed with low-resistivity samples which were doped with phosphorus already during the crystal growth. Fig. 4(b) shows that the reflectance of the low-resistivity samples increases with increasing sample phosphorus concentration (p-doped
bulk, $\sim 10^{19}$ cm$^{-3}$ phosphorus-doped bulk and $10^{20}$–$10^{21}$ cm$^{-3}$ phosphorus-doped emitter) and the Fermi level position. The results hence support the hypothesis of the raised Fermi level and lattice mismatch-induced stress as the explanation for the accelerated Si consumption.

We emphasize that no HF dips were performed between the cleanings in this study. The deterioration of the electrical and optical properties would be further pronounced if each 10 min cleaning sequence was coupled with an HF dip, as is typically done to remove the chemical oxide. Process flows of high-efficiency b-Si solar cells should therefore be carefully designed to avoid unintended Si etching, especially after the phosphorus emitter formation. This may include reducing the solution temperature, cleaning time or eliminating cleaning steps altogether [11, 13].

IV. CONCLUSION

We have shown that heavy phosphorus doping increases the consumption of silicon in the widely used SC1 solution: A high Si etch rate of $\sim 1.4$ nm/min was measured from a planar emitter surface. This is problematic especially for high-efficiency b-Si solar cells, which have a large surface area in contact with the cleaning solution. Sheet resistance of b-Si phosphorus emitters increased from 47 $\Omega$-□ to 57 $\Omega$-□ and 127 $\Omega$-□ during a 10- and 30-min cleaning, respectively. In addition to the altered electrical properties, the optical performance of b-Si suffered from the increased Si consumption. Surface reflectance of the nanotexture increased from 0.9% to 1.7% and 3.3% during 30- and 60-min cleanings, respectively, as a result of reduced nanostructure feature size. Process flows of high-efficiency b-Si solar cells should hence be carefully designed to avoid unintended etching of silicon.

Lastly, we note that unintended etching of highly phosphorus-doped planar and nanotextured silicon can significantly impact theoretical studies seeking to elucidate the impact of different emitter profiles on solar cell performance [36], [37], or, for example, impurity gettering [38]–[42]. Unnecessary cleaning between emitter realization and emitter characterization should therefore be minimized and any HF dips and SC1 cleanings should be carefully reported in such future studies. Moreover, as the effect of cleaning is unexpectedly remarkable, the change in sheet resistance may cause serious reproducibility problems if not enough care is taken to ensure that the cleaning conditions (e.g., time or ratio of chemicals) are kept exactly the same from batch to batch.

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REFERENCES


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