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Impact of Standard Cleaning on Electrical and Optical Properties of Phosphorus-Doped Black Silicon

Toni P. Pasanen, Hannu S. Laine, Ville Vähäniissi, Kristian Salo, Sebastian Husein, and Hele Savin

Abstract—Black silicon (b-Si) has been estimated to considerably grow its market share as a front texture of high-efficiency silicon solar cells. In addition to excellent optical properties, high-efficiency cell process requires extreme cleanliness of the bulk material, and thus cleaning of b-Si surfaces is often a critical process step. While standard clean (SC) 1 solution efficiently removes possible contamination from wafer surfaces, we show here that it may cause challenges in b-Si solar cells. First, the silicon etch rate in SC1 solution is shown to depend on the phosphorous concentration and as high rate as ~ 1.4 nm/min is observed on planar emitter surfaces. When extending the study to b-Si, which has much larger surface area in contact with the cleaning solution, even higher volumetric Si consumption occurs. This is observed in significant changes in emitter doping profiles, for instance, a 10 and 30-min cleaning increases the sheet resistance from 47 to 57 $\Omega/\square$ and 127 $\Omega/\square$, respectively. Furthermore, the SC1 solution alters substantially the nanostructure morphology, which impacts the optics by nearly doubling and more than tripling the surface reflectance after a 30 and 60-min immersion, respectively. Thus, uncontrolled cleaning times may impair both the electrical and optical properties of b-Si solar cells.

Index Terms—Black silicon, etching, nanostructure, phosphorus emitter, RCA clean, standard clean.

I. INTRODUCTION

BLACK silicon (nanostructured silicon, b-Si) is drawing increased interest within the photovoltaic community. The surface texture is able to eliminate reflective losses and is particularly well suited for use with novel diamond wire-sawn multicrystalline wafers, which are unsuited for standard acidic texturing due to the lack of saw damage. Therefore, b-Si has been estimated to substantially grow its industrial market share in the near future [1]. Simultaneously, the PV industry targets

ever higher device efficiencies, which imposes more stringent cleanliness requirements for solar cell processing environments.

A key aspect of process contamination control is wafer surface cleaning prior to high-temperature processing (e.g., emitter formation). This is important especially with specific b-Si fabrication methods, such as metal-assisted chemical etching (MACE) [2], which introduce contaminants that need to be subsequently removed. Possible contamination sources can be efficiently removed from wafer surfaces by standard cleaning (SC, also called RCA clean) [3]. The same solutions are also typically used to precondition silicon surfaces prior to atomic-layer-deposited thin films to enhance surface passivation [4]–[6]. To reduce the consumption of chemicals and costs, the original two-step process can be compressed into a single step by the addition of a complexing agent (e.g., 1,2-cyclohexanediaminetetraacetic acid, CDTA) into a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and water (H_2O) which is known as SC1 solution [7], [8]. The effectiveness of SC1 is based on oxide regeneration on Si surface: NH_4OH dissolves the thin native oxide on silicon at a slow rate, while H_2O_2 simultaneously oxidizes the surface at approximately the same rate [3]. After rinsing in deionized water (DIW), the wafers are usually dipped in diluted hydrofluoric acid (HF) to remove a thin oxide which grows during the cleaning. While this mechanism efficiently removes particles and organic contaminants, it may cause challenges for process design of modern silicon solar cells: Cleaning consumes silicon and hence modifies the surface texture and alters the emitter and the optical properties of the surface. While these changes may be considerable already on planar surfaces, the effect of the cleanings is hypothesized to be even more significant in the case of b-Si as a larger surface area is in contact with the chemicals. Although the duration of a single cleaning step is rather short, the total cleaning time accumulating from several cleanings may be considerably long in a complete cell process.

The consumption of Si in SC1 solution with various compositions has been analyzed in several studies [9]–[14]. The reported etch rates have been ~ 0.8 nm/min for typically used compositions [10]–[12]. However, the studies have not investigated the effect of SC1 on important solar cell parameters, such as the emitter doping profile.

Some studies have also focused on the effect of HF dips on Si consumption. Ebong *et al.* observed an increase in phosphorus emitter sheet resistance and decrease in surface doping concentration after an HF dip, which indicated that considerable amount of Si was removed in the solution [15]. Liu *et al.* studied

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the topic further and discovered that phosphorus concentration affects the etch rate of Si in HF. More specifically, they showed that HF etches phosphorus-doped Si at a surprisingly high etch rate (~ 0.8 nm/min) when the doping concentration is above $3 \times 10^{20} \text{ cm}^{-3}$ [16]. Similar high etch rate in HF has also been reported with heavily arsenic-doped n-type Si [17].

However, it remains ambiguous whether heavy phosphorus doping affects the Si etch rate also in SC1 solution. Furthermore, all past studies have focused only on planar samples, although the surface of a solar cell is always textured, not planar. A surface texture may intensify the effect of the cleanings, and the higher volumetric Si consumption reflect to several important solar cell parameters, such as emitter sheet resistance, morphology of the texture, and the resulting surface reflectance.

In this paper, we investigate the impact of a standard SC1 cleaning solution on silicon consumption using the most typical PV material, i.e., p-type Si with a phosphorus emitter. We give an estimate for the etch rate of phosphorus-doped planar Si in SC1 solution and discuss the physical root cause behind the observed phenomenon. Furthermore, we study the influence of the cleanings on electrical and optical properties of b-Si phosphorus emitters and compare them with p-type b-Si samples without an emitter. Additionally, we expose low-resistivity (0.005–0.01 Ωcm) phosphorus-doped b-Si wafers to the same treatment to confirm that the etching behavior is not only characteristic to a specific doping method.

II. EXPERIMENTAL

Boron-doped p-type Czochralski (CZ) silicon wafers with (100) orientation and a thickness of 525 μm were used in the experiments. First, black silicon was fabricated by deep reactive ion etching (DRIE, Oxford Instruments Plasmalab System 100) to some of the wafers (3–5 Ωcm) using process parameters reported in [18] while the rest of the wafers remained planar (10–15 Ωcm). After an SC1 cleaning and a dip in 1 wt% HF solution, some of the black silicon and planar wafers were introduced into a diffusion furnace (Centrotherm E1200HT 260-4), where an n^+ emitter was formed at 830 $^{\circ}\text{C}$. POCl_3 gas was introduced for 20 min, followed by a 5-min drive-in in oxygen-containing atmosphere. After the phosphosilicate glass was removed by a short 2-min dip in 6 wt% HF solution, initial sheet resistance of the wafers was determined with a four-point probe (Advanced Instrument Technology CMT-SR2000N). The diffusion process resulted in a lower sheet resistance in b-Si wafers (47 $\Omega/\square$) than in the planar counterparts (74 $\Omega/\square$), as expected [19]–[22]. In addition, the electrically active phosphorus concentration profile was determined from a planar sample by electrochemical capacitance-voltage (ECV) profiling (WEP Wafer Profiler CVP21). Doping profile in b-Si was not measured due to instrumental limitations to characterize nanostructures accurately. Since all the wafers were included in a single diffusion run, the initial doping profile in every sample of each type (planar/b-Si) can be assumed to be identical. Subsequently, the wafers were cleaved in quarters for the cleaning experiments.

An SC1 cleaning solution with a composition of $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:1:5$ was prepared from VLSI grade chemicals in a standard way, i.e., ammonia solution (NH_3

25 wt%) was mixed with DIW, and H_2O_2 (30 wt%) was poured into the solution after the batch was heated up to 80 $^{\circ}\text{C}$. A commonly used complexing agent, CDTA, was added to enhance the removal of metal contaminants and the stability of the bath [7], [8], [23]. The b-Si wafer quarters with and without a phosphorus-doped emitter were immersed in the fresh solution for times that varied from one minute to an hour. The samples were rinsed in running DIW and dried with a nitrogen gun immediately after they were lifted from the cleaning bath. No additional H_2O_2 was poured to the solution during the experiment. Another similar bath was then prepared for the planar emitter samples. To exclude the possibility that the etching behavior would be characteristic of POCl_3 -diffused surfaces only, one nanostructured sample of heavily phosphorus-doped CZ-Si (0.005–0.01 Ωcm , 525 μm , (111) orientation) doped during the crystal growth was simultaneously immersed in the same batch for 60 min. Furthermore, to confirm the stability of the cleaning bath, a similar set of planar samples was cleaned in the same one-hour-old cleaning solution directly after the first 60 min etch batch was completed, with no extra H_2O_2 addition. The second batch of planar samples replicated the same sheet resistance values within a 2 $\Omega/\square$ accuracy, confirming that the SC1 solution remained very stable, as previously demonstrated with low metal contamination level or CDTA addition, which both apply to this study [23], [24].

Sheet resistance was measured with a four-point probe from all emitter samples, both planar and b-Si, to quantitatively characterize the change in the amount of dopants. To estimate the etch rate of heavily phosphorus-doped silicon in SC1 solution, sheet resistances were calculated for ECV profiles truncated near the surface [25]. The amount of silicon removed by the cleaning was determined to be the truncation distance that provided the same calculated sheet resistance value as was experimentally measured. In the sheet resistance calculation, a mobility model from Klaassen was employed [26], [27]. The etch rate was then calculated from the amount of silicon removed and the corresponding cleaning time. To confirm the calculated etch rates, ECV profiles were measured on planar samples cleaned for 10 and 30 min and compared with the original profile. The samples were then dipped in 1 wt% HF until the surface turned hydrophobic (40 s) to reveal a bare Si surface under the thin chemical oxide. The HF dip was kept short enough to prevent additional Si etching after the SC1 cleaning. The evolution of the nanostructure was characterized by integrating sphere-based surface reflectance measurements (Agilent Cary 5000) and SEM imaging (Zeiss Supra 40).

III. RESULTS AND DISCUSSION

A. Etch Rate

Fig. 1 shows the electrically active phosphorus profiles and the corresponding sheet resistance (R_{sh}) values, as measured by four-point probe, of planar samples prior to any cleanings or after SC1 immersion for various times. The sheet resistance values demonstrate a significant reduction in phosphorus concentration with increasing cleaning time, indicating that the surface is indeed etched by the cleaning chemicals. Comparison of the experimentally determined sheet resistance and the

Fig. 1. Electrically active phosphorus profiles of planar samples prior to any cleanings and after 10- or 30-minute cleaning determined by ECV profiling. Corresponding experimentally determined sheet resistance values (R_{sh}) are shown in the legend. The profiles of the cleaned samples are offset by the calculated etch depths. Surface regions which were removed by 10-, 30- and 60-min SC1 cleanings are highlighted.

Fig. 2. Sheet resistance of b-Si and planar emitter samples after the immersion in SC1 cleaning solution for various times between 1 min and 1 h. Note the logarithmic y-axis. The lines act as a guide for the eye. The error estimates are based on a 15 s uncertainty in cleaning time and the variation range of the measured sheet resistance.

corresponding values calculated for the truncated initial profiles imply that 10-, 30- and 60-min cleanings consumed 14 ± 1.5 , 36 ± 1.3 , and 71 ± 1.3 nm from the sample surface, respectively. The removed regions are highlighted in Fig. 1. Hence, the etch rate of Si was as high as 1.4 ± 0.3 nm/min on average during the first 10 min and slowed down to 1.2 ± 0.2 nm/min for the last 30 min of the 60-min cleaning. The uncertainty results from a 15 s uncertainty in cleaning time, the standard deviation of the sheet resistance measurement ($\sim 1 \Omega/\square$), and a 5% uncertainty in the ECV data. The determined etch rate is significantly higher than ~ 0.8 nm/min previously reported for lightly doped surfaces [10]. The ECV profiles measured from the cleaned samples and offset by the calculated etch depths fit well to the original phosphorus profile, which confirms the calculated etch rates. The slight deviation between the profiles of the 0 and 30-min cleaned samples in the region deeper than ~ 170 nm can be attributed to the reduced accuracy of the ECV profiling method for low doping concentrations.

Fig. 3. Scanning electron microscope images of the nanostructures with and without a POCl_3 emitter after various SC1 cleaning times. All images are presented at the same scale, indicated by the scale bar.

The decrease in etch rate as the etching proceeds coincides with a reduced surface phosphorus concentration. Hence, the accelerated Si consumption could be explained by the increased Fermi level which reduces the activation energy required to release an Si atom from the lattice, as in the case of HF [16], [17]. This explanation implies that heavy boron doping would reduce the etch rate as the Fermi level is shifted toward the valence band. However, as the etch rate starts to decrease already after the first 10 min, while the electrically active surface phosphorus concentration remains rather constant for the following 20 min, inactive phosphorus could be another explanation for the accelerated Si consumption. The applied diffusion process is known to result in a considerable amount of inactive phosphorus near the surface, which is not visible in the ECV profile [22]. Hence, also crystal defects (e.g., precipitated phosphorus) could contribute to the accelerated Si consumption. Alternatively, the consumption of silicon could be intensified by lattice mismatch-induced stress in the heavily phosphorus-doped region [16].

B. Electrical Properties of Black Silicon Emitters

Since SC1 solution was found to etch planar silicon surfaces at an unexpectedly high rate, the corresponding impact on b-Si phosphorus emitters and their electrical properties can be assumed to be even higher. Consequently, Fig. 2 compares the sheet resistance of the b-Si and planar phosphorus emitter samples immersed in SC1 solution as a function of immersion time. The b-Si samples have a higher initial phosphorus dose indicated by the lower sheet resistance, which is caused by the larger surface area of the nanostructures. As hypothesized, the sheet resistance of the b-Si samples increases with a slightly higher rate compared with planar surfaces. This behavior can be explained by the b-Si spikes having a larger area in contact with the cleaning solution, which increases the volumetric Si consumption and underscores the need to optimize cleaning procedures particularly in b-Si solar cells. The relative difference between the sheet resistance of b-Si and planar samples diminishes with increasing cleaning time as the extremely heavily doped layers at the nanostructure surface are removed.

After a 30-min immersion, corresponding to three standard 10-min cleanings, which can plausibly be included in a research-scale high-efficiency solar cell process flow, the sheet resistance nearly triples in the b-Si samples. This change would result in

Fig. 4. (a) Reflectance spectra of b-Si POCl₃ emitter samples before and after the immersion in SC1 cleaning solution for various times between 10 and 60 min. (b) Reflectance of p-type samples with and without a POCl₃ emitter and low-resistivity n-type samples before and after a 60-min cleaning. The solar spectrum weighted average reflectances are calculated between 280 and 1000 nm.

increased resistive losses in the emitter and deterioration of Ohmic contacts, resulting in a significantly reduced cell efficiency.

C. Surface Morphology and Reflectance

In addition to electrical properties, surface morphology and the resulting optics are essential parameters for high-efficiency solar cells. Therefore, the impact of the observed high Si consumption in SC1 solution on these properties is further investigated. Fig. 3 presents the evolution of the POCl₃ diffusion-doped b-Si structures in SC1 solution. The SEM images describe separate samples cleaved from a single wafer after the b-Si fabrication and subsequent diffusion. Corresponding images of p-type b-Si without an emitter are shown for reference. In the phosphorus-doped nanostructure, some modifications can already be seen after a 10-min immersion. The change is more significant after a 30- or 60-min cleaning as expected based on the sheet resistance results. Although none of the DRIE-fabricated b-Si spikes is perfectly identical with each other, which is one of the reasons for the excellent optical properties of b-Si [28], the initial nanostructures can be assumed to have been similar on average over a large area in all wafers.

To investigate how the reduction in nanostructure feature size affects the optical properties of b-Si, surface reflectance was next measured from the same samples. Fig. 4(a) presents the surface reflectance spectra of the b-Si emitter wafers. The reflectance increases considerably with increasing SC1 cleaning time: The solar spectrum weighted average reflectance increases from 0.9% to 1.7% and 3.3% during a 30- and 60-min cleaning, respectively. Especially, the deterioration of optical properties is pronounced in the ultraviolet range where a 30-min cleaning doubles and a 60-min cleaning quintuples the peak reflectance at 280 nm wavelength from 3.7% to 8.1% and 18.4%, respectively. The loss of surface antireflectivity hence confirms the changes in the nanostructure morphology which were observed with SEM imaging. Since advanced atomic-layer-deposited thin films have solved the issue of extensive surface recombination

in nanostructures with large surface area and high aspect ratio [18], [29]–[32], the reduction of nanostructure size should not particularly promote more efficient surface passivation. In high-efficiency b-Si solar cells, the increased reflectance would thus directly impair the short-circuit current and hence cell efficiency.

Some b-Si surfaces, such as those fabricated by laser-treatment [33] or MACE [34], are typically smoothed by wet chemical etching, which results in increased surface reflectance. After this treatment, the effect of SC1 cleaning on the initially larger reflectance may be weaker than demonstrated here. However, it will not remove the fact that subsequent SC1 cleanings, which are preferred, e.g., prior to atomic layer deposition of surface passivation thin films [4]–[6], affect the electrical properties of phosphorus-doped emitters with an amount larger than previously expected even on planar surfaces.

Fig. 4(b) shows how phosphorus doping concentration affects the behavior of b-Si reflectance under immersion in SC1 solution. Also in the emitterless case, the reflectance increases by immersion in the cleaning solution. However, the increase is more pronounced in the POCl₃ emitter samples. This observation is supported by the SEM images in Fig. 3, which reveal that the features of POCl₃-doped b-Si have changed more drastically compared with the sample with no emitter during a 60-min immersion. Indeed, the 45-min POCl₃ sample reflects more than the 60-min p-type sample without an emitter. The slight difference in the initial UV range spectra is due to minor differences in the nanostructures caused by the diffusion process. The low reflectance of the low-resistivity samples in the infrared range (wavelengths beyond 1000 nm) is caused by free-carrier absorption [35].

The reflectance spectra in Fig. 4(b) support the observation of heavy phosphorus-doping induced increased Si consumption. Furthermore, the observed phenomenon is not only a feature of POCl₃-diffused surfaces since a similar behavior is observed with the low-resistivity material which was doped with phosphorus already during the crystal growth. Fig. 4(b) shows that the reflectance of the 60-min samples increases with increasing sample phosphorus concentration (p-doped

bulk, $\sim 10^{19} \text{ cm}^{-3}$ phosphorus-doped bulk and $10^{20} - 10^{21} \text{ cm}^{-3}$ phosphorus-doped emitter) and the Fermi level position. The results hence support the hypothesis of the raised Fermi level and lattice mismatch-induced stress as the explanation for the accelerated Si consumption.

We emphasize that no HF dips were performed between the cleanings in this study. The deterioration of the electrical and optical properties would be further pronounced if each 10-min cleaning sequence was coupled with an HF dip, as is typically done to remove the chemical oxide. Process flows of high-efficiency b-Si solar cells should therefore be carefully designed to avoid unintended Si etching, especially after the phosphorus emitter formation. This may include reducing the solution temperature, cleaning time or eliminating cleaning steps altogether [11], [13].

IV. CONCLUSION

We have shown that heavy phosphorus doping increases the consumption of silicon in the widely used SC1 solution: A high Si etch rate of $\sim 1.4 \text{ nm/min}$ was measured from a planar emitter surface. This is problematic especially for high-efficiency b-Si solar cells, which have a large surface area in contact with the cleaning solution. Sheet resistance of b-Si phosphorus emitters increased from $47 \text{ } \Omega/\square$ to $57 \text{ } \Omega/\square$ and $127 \text{ } \Omega/\square$ during a 10- and 30-min cleaning, respectively. In addition to the altered electrical properties, the optical performance of b-Si suffered from the increased Si consumption. Surface reflectance of the nanotexture increased from 0.9% to 1.7% and 3.3% during 30- and 60-min cleanings, respectively, as a result of reduced nanotexture feature size. Process flows of high-efficiency b-Si solar cells should hence be carefully designed to avoid unintended etching of silicon.

Lastly, we note that unintended etching of highly phosphorus-doped planar and nanotextured silicon can significantly impact theoretical studies seeking to elucidate the impact of different emitter profiles on solar cell performance [36], [37], or, for example, impurity gettering [38]–[42]. Unnecessary cleaning between emitter realization and emitter characterization should therefore be minimized and any HF dips and SC1 cleanings should be carefully reported in such future studies. Moreover, as the effect of cleaning is unexpectedly remarkable, the change in sheet resistance may cause serious reproducibility problems if not enough care is taken to ensure that the cleaning conditions (e.g., time or ratio of chemicals) are kept exactly the same from batch to batch.

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REFERENCES

- [1] *International Technology Roadmap for Photovoltaic: Results 2016*, 8th ed., Mar. 2017.
- [2] S. Koyunov, M. S. Brandt, and M. Stutzmann, "Black nonreflecting silicon surfaces for solar cells," *Appl. Phys. Lett.*, vol. 88, May 2006, Art. no. 203107.
- [3] W. Kern and D. A. Puotinen, "Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology," *RCA Rev.*, vol. 31, pp. 187–206, 1970.
- [4] M. Li *et al.*, "Effect of surface pretreatment in the thermal atomic layer deposition of Al_2O_3 for passivation of crystal Si solar cells," *Jpn. J. Appl. Phys.*, vol. 53, Jul. 2014, Art. no. 08LC04.
- [5] Y. Bao, S. Li, G. von Gastrow, P. Repo, and H. Savin, "Effect of substrate pretreatments on the atomic layer deposited Al_2O_3 passivation quality," *J. Vac. Sci. Technol. A*, vol. 33, Nov. 2014, Art. no. 01A123.
- [6] G. Kaur *et al.*, "Understanding surface treatment and ALD AlO_x thickness induced surface passivation quality of c-Si Cz wafers," *IEEE J. Photovolt.*, vol. 7, no. 5, pp. 1224–1235, Sep. 2017.
- [7] E. I. Cooper *et al.*, "Method for cleaning semiconductor devices," U.S. Patent 5962384, Oct. 1999.
- [8] G. W. Gale *et al.*, "Enhancement of semiconductor wafer cleaning by chelating agent addition," *J. Electrochem. Soc.*, vol. 148, pp. G513–G516, Aug. 2001.
- [9] J. E. A. M. van den Meerakker and M. H. M. van der Straaten, "A mechanistic study of silicon etching of $\text{NH}_3/\text{H}_2\text{O}_2$ cleaning solution," *J. Electrochem. Soc.*, vol. 137, pp. 1239–1243, Apr. 1990.
- [10] T. Ohmi, M. Miyashita, and T. Imaoka, "Foresightedness in RCA cleaning concept and importance of surface microroughness in ULSI device performance," in *Proc. Microcontamination 91 Conf. Expo.*, San Jose, CA, USA, Oct. 1991, pp. 491–510.
- [11] H. Kobayashi, J. Ryuta, T. Shingyouji, and Y. Shimanuki, "Study of Si etch rate in various composition of SC1 solution," *Jpn. J. Appl. Phys.*, vol. 32, pp. L45–L47, Jan. 1993.
- [12] P. Boelen *et al.*, "Optimization of dilute SC1," in *Proc. 5th Int. Symp. Cleaning Technol. Semicond. Device Manuf.*, J. Ruzyllo and R. E. Novak, eds., Mar. 1998, Electrochem. Soc., vol. 97–35, pp. 161–167.
- [13] K. Yamamoto, A. Nakamura, and U. Hase, "Control of cleaning performance of an ammonia and hydrogen peroxide mixture (APM) on the basis of a kinetic reaction model," *IEEE Trans. Semicond. Manuf.*, vol. 12, no. 3, pp. 288–294, Aug. 1999.
- [14] G. K. Celler, D. L. Barr, and J. M. Rosamilia, "Etching of silicon by the RCA standard clean 1," *Electrochem. Solid-State Lett.*, vol. 3, pp. 47–49, Nov. 2000.
- [15] A. Ebong *et al.*, "High efficiency inline diffused emitter (ILDE) solar cells on mono-crystalline CZ silicon," *Prog. Photovolt., Res. Appl.*, vol. 18, pp. 590–595, May 2010.
- [16] L. Liu, F. Lin, M. Heinrich, A. G. Aberle, and B. Hoex, "Unexpectedly high etching rate of highly doped n-type crystalline silicon in hydrofluoric acid," *ECS J. Solid State Sci. Technol.*, vol. 2, pp. P380–P383, Jul. 2013.
- [17] N. Valckx *et al.*, "Study of the etching mechanism of heavily doped Si in HF," *Solid-State Phenom.*, vol. 187, pp. 41–44, Apr. 2012.
- [18] P. Repo *et al.*, "Effective passivation of black silicon surfaces by atomic layer deposition," *IEEE J. Photovolt.*, vol. 3, no. 1, pp. 90–94, Jan. 2013.
- [19] J. Oh, H.-C. Yuan, and H. M. Branz, "An 18.2%-efficient black-silicon solar cell achieved through control of carrier recombination in nanostructures," *Nature Nanotechnol.*, vol. 7, pp. 743–748, Sep. 2012.
- [20] B. Kafle *et al.*, "On the emitter formation in nanotextured silicon solar cells to achieve improved electrical performances," *Sol. Energy Mater. Sol. Cells*, vol. 152, pp. 94–102, Aug. 2016.
- [21] G. von Gastrow *et al.*, "Recombination processes in passivated boron-implanted black silicon emitters," *J. Appl. Phys.*, vol. 121, May 2017, Art. no. 185706.
- [22] T. Pasanen, V. Vähänissi, N. Theut, and H. Savin, "Surface passivation of black silicon phosphorus emitters with atomic layer deposited $\text{SiO}_2/\text{Al}_2\text{O}_3$ stacks," *Energy Procedia*, vol. 124, pp. 307–312, Sep. 2017.
- [23] H. Saloniemi, T. Visti, S. Eränen, A. Kiviranta, and O. Anttila, "Improvement of SC-1 bath stability by complexing agents," *Phys. Scripta*, vol. 2002, pp. 226–229, 2002.
- [24] H. F. Schmidt *et al.*, " H_2O_2 decomposition and its impact on silicon surface roughening and gate oxide integrity," *Jpn. J. Appl. Phys.*, vol. 34, pp. 727–731, Feb. 1995.
- [25] K. McIntosh and M. Abbott, "PV Lighthouse: Sheet resistance calculator," [Online]. Available: <https://www2.pvlighthouse.com.au/calculators/sheet%20resistance%20calculator/sheet%20resistance%20calculator.aspx>. Accessed on: Aug. 14, 2017.
- [26] D. B. M. Klaassen, "A unified mobility model for device simulation – I. Model equations and concentration dependence," *Solid-State Electron.*, vol. 35, pp. 953–959, Jul. 1992.

- [27] D. B. M. Klaassen, "A unified mobility model for device simulation – II. Temperature dependence of carrier mobility and lifetime," *Solid-State Electron.*, vol. 35, pp. 961–967, Jul. 1992.
- [28] A. J. Bett *et al.*, "Wave optical simulation of the light trapping properties of black silicon surface textures," *Opt. Express*, vol. 24, pp. A434–A445, Jan. 2016.
- [29] M. Otto *et al.*, "Extremely low surface recombination velocities in black silicon passivated by atomic layer deposition," *Appl. Phys. Lett.*, vol. 100, May 2012, Art. no. 191603.
- [30] W.-C. Wang *et al.*, "Surface passivation of efficient nanotextured black silicon solar cells using thermal atomic layer deposition," *ACS Appl. Mater. Interfaces*, vol. 5, pp. 9752–9759, Sep. 2013.
- [31] B. Dou *et al.*, "Surface passivation of nano-textured silicon solar cells by atomic layer deposited Al_2O_3 films," *J. Appl. Phys.*, vol. 114, Nov. 2013, Art. no. 174301.
- [32] G. von Gastrow *et al.*, "Analysis of the atomic layer deposited Al_2O_3 field-effect passivation in black silicon," *Sol. Energy Mater. Sol. Cells*, vol. 142, pp. 29–33, 2015.
- [33] S. Koyunov, M. S. Brandt, and M. Stutzmann, "Black multi-crystalline silicon solar cells," *Phys. Status Solidi Rapid Res. Lett.*, vol. 1, pp. R53–R55, Oct. 2007.
- [34] B. K. Nayak, V. V. Iyengar, and M. C. Gupta, "Efficient light trapping in silicon solar cells by ultrafast-laser-induced self-assembled micro/nano structures," *Prog. Photovolt., Res. Appl.*, vol. 19, pp. 631–639, Jan. 2011.
- [35] S. C. Baker-Finch, K. R. McIntosh, D. Yan, K. C. Fong, and T. C. Kho, "Near-infrared free carrier absorption in heavily doped silicon," *J. Appl. Phys.*, vol. 116, pp. 063106:1–063106-12, Aug. 2014.
- [36] B. Min *et al.*, "Heavily doped Si:P emitters of crystalline Si solar cells: Recombination due to phosphorus precipitation," *Phys. Status Solidi Rapid Res. Lett.*, vol. 8, pp. 680–684, Jun. 2014.
- [37] H. Wagner *et al.*, "Optimizing phosphorus diffusion for photovoltaic applications: Peak doping, inactive phosphorus, gettering, and contact formation," *J. Appl. Phys.*, vol. 119, pp. 185704-1–185704-9, May 2016.
- [38] V. Vähänissi, A. Haarahiltunen, H. Talvitie, M. Yli-Koski, and H. Savin, "Impact of phosphorus gettering parameters and initial iron level on silicon solar cell properties," *Prog. Photovolt., Res. Appl.*, vol. 21, pp. 1127–1135, Aug. 2013.
- [39] S. P. Phang and D. Macdonald, "Effect of boron cooping and phosphorus concentration on phosphorus diffusion gettering," *IEEE J. Photovolt.*, vol. 4, no. 1, pp. 64–69, Jan. 2014.
- [40] A. Peral, A. Dastgheib-Shirazi, H. Wagner, G. Hahn, and C. del Cañizo, "Effect of electrically inactive phosphorus versus electrically active phosphorus on iron gettering," *Energy Procedia*, vol. 77, pp. 311–315, Aug. 2015.
- [41] H. S. Laine *et al.*, "Impact of iron precipitation on phosphorus-implanted silicon solar cells," *IEEE J. Photovolt.*, vol. 6, no. 5, pp. 1094–1102, Jun. 2016.
- [42] E. Cho *et al.*, "Comparison of POCl_3 diffusion and phosphorus ion-implantation induced gettering in crystalline Si solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 157, pp. 245–249, Dec. 2016.

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